

## Lead-Free Reflow Oven Parameter Optimization

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### Abstract

Because of the potential danger that Lead poses to human health, Parliament of the European Union approved a law to take effect on July 1, 2006 which forbids the use of lead in electrical and electronic products. As a result, manufacturers throughout the world started to look into replacing lead-based solder with lead-free pastes using a combination of alloys. During this transition, many issues have been found related to the reliability of the solder joints under a lead-free process. One of the findings is the solder cold joints effect produced by this new alloy that can potentially have a major impact on the reliability of electronic systems. Two major factors, conveyor tunnel speed, and different melting temperatures, need to be fully investigated to optimize the production process of using lead-free solder pastes.

Our research emphasizes the impact of these two major parameters on the lead-free production process. The investigation is conducted through a designed experiment considering the afore-mentioned factors by using two different conveyor speeds treated under different levels of temperatures.

Raw testing data were gathered from a reflow oven and appropriate statistical analysis will be performed to help identify optimal settings of reflow oven parameters. The results can potentially help improve manufacturing processes and productivity.

This article presents our preliminary research results of using lead-free solder paste in an electronic production line at different temperatures and conveyor speeds. This is part of the problematic implementation of RoHS (Reduction of Hazardous Substances).

## Introduction

Lead or any of the six other hazardous materials (lead, mercury, cadmium, chromium, (Polybrominated Biphenyls) PBBs and (Polybrominated Diphenyl Ether) PBDEs present a problem to human health, therefore Governments throughout the world and other non-government agencies have been considering regulating its use for some time. The initiative originated with the European Union and in 2003. The E.U. Parliament approved a law that took effect on July 1, 2006 forbidding the use of lead in electronic products.

Although the benefits are quite clear, the consequences or side-effects are not.

Substances should not be banned without scientific analysis of risk trade-offs and without full consideration of consequences to both manufacturers and consumers. [1]

As a result, manufacturers throughout the world started to look into replacing the use of lead-based solder with lead-free paste using a combination of alloys.



Figure 1 The new logo representing RoHS and Lead-Free products. [2]

Lead-free has been in development for more than 15 years [3]. Much research has been done in terms of low temperature alloy, [4] electronic waste and related health issues [5], reflow oven usage within a controlled temperature window [6], solder pastes and joints [7] [8], Tin Whisker effect [9], Nitrogen effect [10] air bath processes [11] [12], and cleaning up processes [13].

Investigation on the elimination of lead is still a work in process for the electronic industry throughout the world. Some of the results have lead to changes in the production processes, however most industries are rather cautiously in proceeding with full implementation. The long term effect is still an unknown factor to consider.

All members of the European Union are bound by the initiative, but a number of them have requested special exceptions based on economic impact and lead-free component availability. California is in the process of adopting similar laws applying to the reduction of hazardous substances as well as China, Japan and others.

Although there are no laws in the U.S. similar to RoHS in Europe, all organizations concerned in establishing standards—Underwriters Laboratories, Canadian Standards Association, National Electrical Manufacturer Industries—are involved in the process of writing norms that will lead to the implementation of lead-free certification.

One of the concerns is the possible premature failure of each assembly and/or the components due to strain. Based on the research, a report was issued that indicates the minimum number of IST (Interconnect Stress Failures) cycles-to-failure recommended for the different industries [14].

The recommendation is graphically presented in Figure 1.

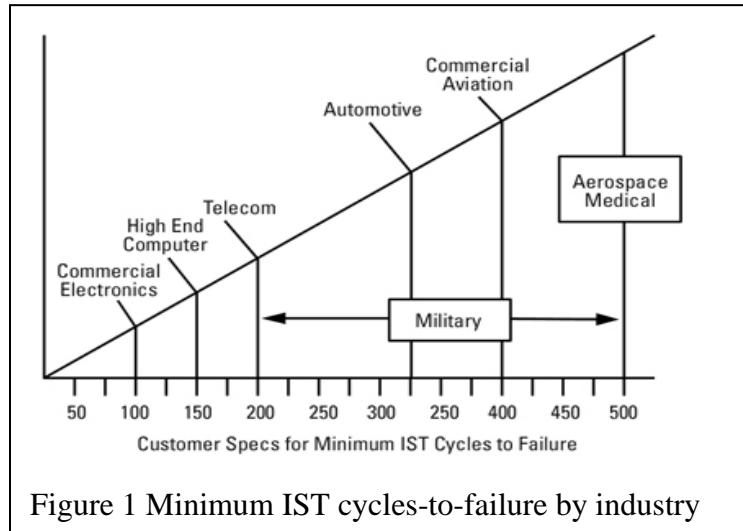


Figure 1 Minimum IST cycles-to-failure by industry

## Research Objectives

Our investigation is to determine the best profile for two factors and two levels with three replications.

1. Temperature at two levels, low (240° C/464°F) and high 260°C (500°F).
2. Conveyor speed at (low) 0.35 fpm (feet per minute) and (high) 0.50 fpm.

There are three variable responses used to determine the quality of the process:

1. Cold joints or voids.
2. Thermal effect or apparent damage to components.
3. Quality of all solder joints in the (Printed Circuit Board) PCBs.

The other factors are to remain constant. By using the above combinations, a randomized experiment is replicated three times to obtain the data given after each treatment and creating the (Analysis of Variance) ANOVA table.

One of the important responses (tin-whiskers) to look for, requires an extended amount of time of exposure under a controlled environment to produce any results, therefore this investigation will not be able to report on that effect.

In addition to the above, the following factors were also taken into account before our experiment was designed.

1. Composition of paste (type of alloy).
2. Type of flux.
3. Population of the board, more or less dense.
4. Temperatures in zones 1, 2 and 3.
5. Cooling rate on zone 4; too fast, frozen joints; too slow, an overexposure.
6. Cyclonic speed and volume of air that moves in each zone.
7. Different temperatures and conveyor speeds are just two of the many variables.

## **The Hardware and Collection of Data**

Our (Design of Experiment) DOE involves one reflow oven, lead-free solder paste, and fourteen PCBs populated with the necessary components. Two people were involved, the student and one assistant.

Previous knowledge of this operation is a must and the ability to predict results from the response variables based on previous experiences is also valuable.

The first step taken was to prepare the oven by setting it up with the first profile. Since it is advisable to operate the oven at the desired and stable temperature, one hour is allowed for this process to take place.

The second most important step is to prepare the PCBs, but first the solder should be removed from the refrigerator where it is kept at a controlled temperature and allowed to reach the ambient temperature.

The stencil should also be prepared with the solder paste to screen the PCBs by spreading an even, thin layer with a squeegee over the surface of the boards and allowing it to dry before proceeding to the next operation.

Once the PCBs are screened with the lead-free solder paste, they must be populated with the (Surface Mount Devices) SMDs. This is achieved by a pick and place machine. As soon as this step is completed, then the boards are ready to be placed in the oven that by now should show stable temperature readings and cooling fans running.

After a couple of trial runs, the experiment was run and data were collected. Original experimental data is shown in Table 1.

A total of 14 boards were prepared for the experiment, however only the data obtained on 12 boards—numbered from 1 to 12—were used for statistical purposes. Two PCBs out of the 14 were used in the trial run. These two boards, although data was collected, are not part of the statistical experiments.

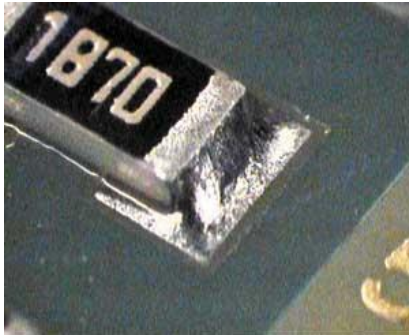
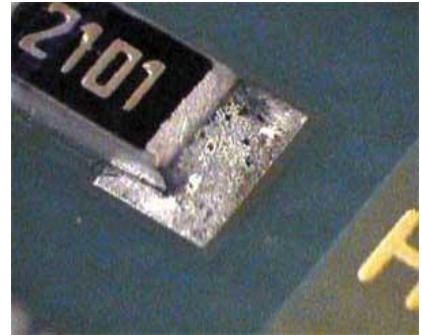


Figure 2 on the left shows a sample of lead-based joint, while the Figure 3 on the right displays a lead-free joint.



Profile	Oven Settings	Cold Joint Defects	High 1-Low 5 Joint Q. 1-5	Effect Thermal	PC Board#
1	Low Temp	1	3	1	1
	Slow Conv.	1	2	1	2
	PCB 1-3	2	1	2	3
2	Low Temp	2	4	2	4
	Fast Conv.	3	5	2	5
	PCB 4-6	1	3	2	6
3	High Temp	1	1	1	7
	Slow Conv.	2	2	1	8
	PCB 7-9	0	2	1	9
4	High Temp	2	3	1	10
	Fast Conv.	0	1	1	11
	PCB 10-12	3	3	1	12

Table 1 Responses of all Variables



Figure 4 Reflow oven similar to the one where the experiments were conducted.

### Data Analysis

In order to evaluate the process effect of the different variables, ANOVA was performed and the  $F$  statistics obtained. The following are the statistical results obtained with ANOVA using Excel software.

From the  $F$  distribution table, the  $F$ -critical value with 3  $df$  for the numerator and 8  $df$  for the denominator at the  $\alpha$  of 0.05 level is 4.07 which is larger than the  $F$  critical value of 3.008 obtained in the ANOVA table above. Therefore we reject the null hypothesis that sample mean response is the same for all PCBs.

Table 2 Summary of Results

Response			Results						
			Source	SS	df	MS	F	P-value	F crit
Variables	Average	Total							
Cold Joints	1.5	18	Sample	10.4444	3	3.4815	4.8205	0.0091	3.0088
PCB Quality	2.5	30	Columns	9.5556	2	4.7778	6.6154	0.0051	3.4028
Thermal Effects	1.3	16	Interaction	2.8889	6	0.4815	0.6667	0.6772	2.5082

Figure 2 displays the plotted results for all PCBs using the four oven profiles. The average of the boards tested shows that the solder joints quality in lead-free soldering is a major level of rejection.

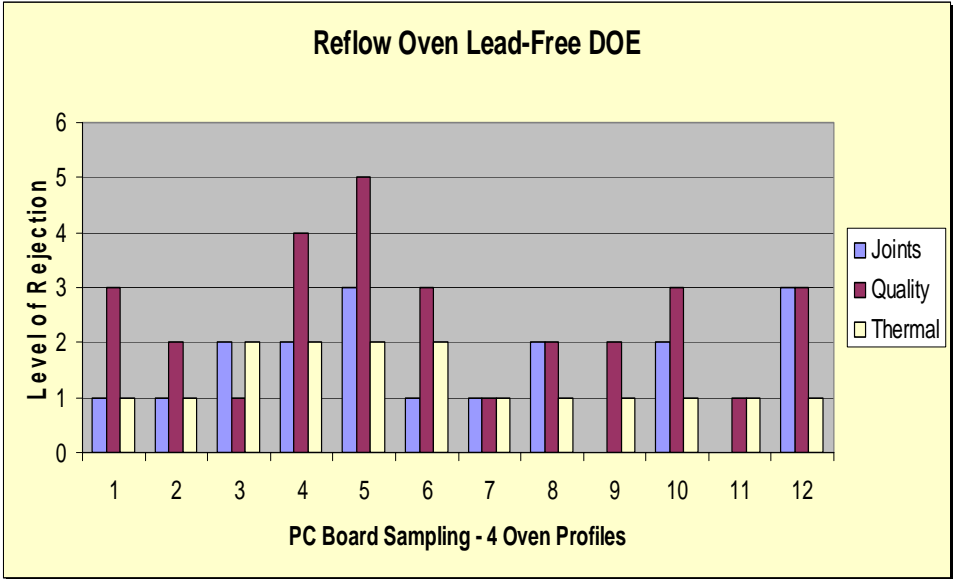


Figure 5 Summary of Experimental Data

## **Conclusions and Recommendations**

The elimination of lead in the electronic and other associated industries is necessary; however our experiment has shown that a lead-free solder joint does not produce the same joint quality as with the lead-based paste, although an improvement is possible by using a combination of different alloys.

Our research and experiment lead us to conclude that the joints' stress factor on a long term basis should be considered. Temperature, humidity, vibration and strain are some of the most important issues to observe closely.

An experiment takes time, not to mention technical and human resources. A profile for the best results must include optimization related to production. The cost of compliance can reach un-fordable numbers for most small manufacturers, to that additional expenses must be added, such as the cost of new equipment, training personnel and higher lead-free component cost.

We highly recommend that no short cuts should be taken in this type of research. A more concerted effort by the industry, educational institutions and governments must take place. This is the only way that the goals of a lead-free and safe product will eventually be a reality.

## **Discussions and Future Work**

As stated in our conclusions, further studies are necessary, but should include more factors, such as all temperature zones; wetting force and time; more than two conveyor speeds; ramp-down and cooling off period; air circulation; different lead-free solder pastes and more.

Furthermore, specific profiles for PCB size and component population for the different models to be manufactured should be established. Also more responses are required: functional tests with adequate equipment, evaluation after a two weeks aging process under a controlled environment, and so forth.

Changing from a lead-based production to a lead-free is a multifaceted and costly process. All industries trying to migrate to lead-free will find that it is a process which many are discovering more complex than initially anticipated.



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## Biography

MANUEL MIRA received the A. S. degree in Electronics (1954) from National Schools, Brazil. He received the B.S.I.T, Information Technology (2004) from Barrie University, Miami, Florida. Currently is a graduate student at the Engineering School of Technology at Western Carolina University. He is a member of the SME and IEEE.

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