The Design and Implementation of Multiple Processors in Control of Multiple High Power DC Motors

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I. Abstract

Small microcontrollers are popular and easy to use in all kinds of applications. On the other hand, they are also limited in their capacity of inputs/outputs (I/Os), internal peripherals, and external interfacing. In order to extend the capabilities of pre-developed modules, the use of these small microcontrollers must be linked as individual modules through a central control format to accommodate the special needs of a complex project. A serial link between all the modules that uses well defined protocols is essential to the success of project implementation in an efficient and economical way.

Using microprocessor/microcontroller in various control applications is not only one of the major topics in Engineering Technology curricula, but also of interest in industry applications. The control of multiple high power DC motors in the range of 10 Amps or above with multiple small microcontrollers poses an interesting and challenging task in design. The implementation and test of the design is also demanding. The solutions, to serially linked multiple microcontroller modules and their controls of high power DC motors, are the focuses of this article

II. Introduction

An assignment was given to the authors, while doing an application project sponsored by a private industry, outside of the university. The task was to design an automated control circuit that uses a microprocessor/microcontroller to control multiple, high power, DC motors (10 DC motors running at 10A-15A) with user selectable options for various motor actions. The project goals are: keep the control simple, independent, and low cost in manufacturing.

The selected design approach is to modulate a design that uses a popular 8 bit PIC16F84A [1] microcontroller to control a DC motor, and link each module through specialized protocols between the modules and the central command controller responsible for communications between the system and the end user.

An additional focus of this project is the use of a high power DC motor control circuit with a special heat sink design and noise suppressor circuit that minimizes the noise contamination while running the DC motors in high speed and continuous formats. The test and selection of proper components to minimize the noise contamination is also implemented.

This practical project design, development, and testing have not only put the faculty expertise in use to assist the local industry needs but the most import of all is that triggered the students' interest and challenged their learning attitude and made them high motivated in class/lab material.

III. The Designs

To achieve a low cost and simple solution to the control of multiple high power DC motors, the simple PIC 16F84A [2], [3] microcontroller is designated to meet this goal. The first step is to design a modular circuit that uses the minimum resources of this processor to control a DC motor's speeds and directions. This module has to be fully tested and proven effective in controlling a single DC motor. The second step is to design a protocol link that uses the available resources of the controller to conduct the necessary communications between different modules of control through a variety of actions associated with the motors. The third step is to test the integrity of the communication protocols to ensure there is no miscommunication or unanticipated behavior in the controlled motors.

Although the hardware design appears complex, it has a lot of duplication due to multiple CPUs in the system. There are four major parts in this design: (1) the single master that handles the user's commands and communications via keypad and LCD module, (2) the multiple slaves that actual generate the PWM signals to drive the motors, (3) a simple three wires serial links between a single master and multiple slaves and two wires framing controls, and (4) the multiple motor driver circuits that have special heat sinks for handling the high current and filters for suppressing the brush DC motors' noise contaminations.

1. Master Control Circuit

The master interface circuit has a standard 4x4 keypad, a LCD module, a shift register, and three software controlled I/Os for the serial interface buses to the slave CPUs.

The keypad is direct interfaced to PORTB RB0-RB7 with eight 10K pull up resistors [1], [2]. RB0 (IO_1) and RB1 (IO_2) are dually used for the slaves' serial communication framing I/O controls. These two logic lines generate four different states that are used as guidance to the slaves to follow the predefined protocols. RB2 (MA_E) is also used as a control of the slave's de-multiplexer enable (marked as MA_E/RB2) that serves as an alarm condition for the master to shut down all the motors when an emergency condition is encountered.

The LCD module is connected to a 74164 shift register [4] in a parallel format, but its interface to the CPU is in a serial form. This is needed because of the limited number of available I/Os on the master CPU. RA2 (LCD_E) and RA3 (LCD_RS) are used for E and RS controls on the LCD display module [5].

The entire serial interface is done through PORTA. RA0 (marked as CLK) is used to generate the clock, RA1 (marked as DOUT) is the control data output from a master to the slaves, and RA4 (marked as DIN) is a return data line from the slaves to a master. RA4 is an open drain I/O. Its required pull up resistor (10K) connection makes it the best choice for this type of interface communication [1], [2]. There are three serial communication lines that are not only used in master-slave configuration, but also in CPU-LCD interactions. There is no unused pin on the master circuit. Figure 1 presents the master hardware circuit design.

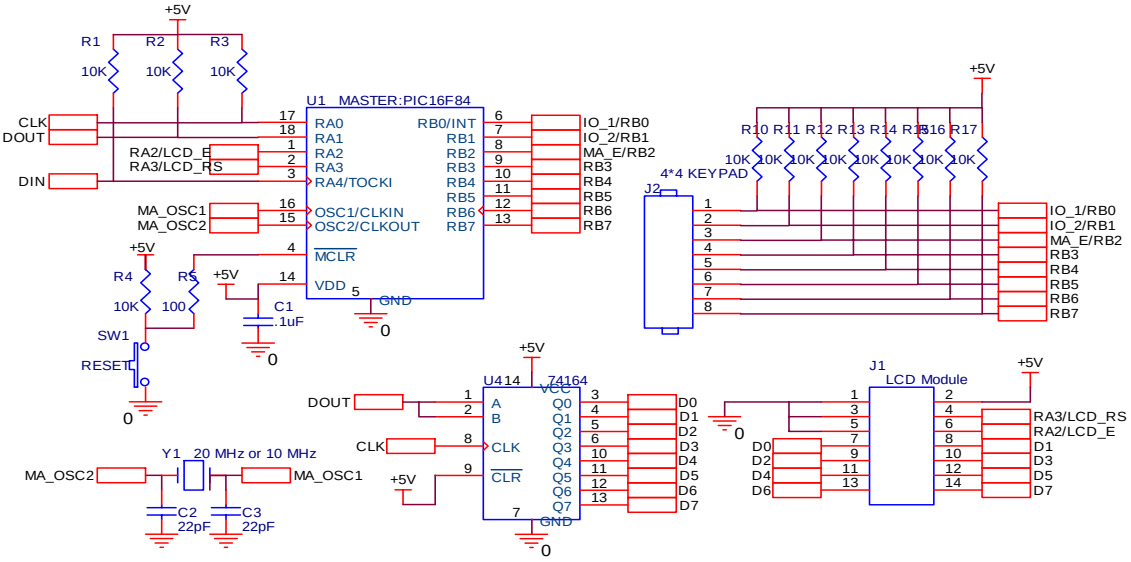

Figure 1: The Master Hardware Circuit

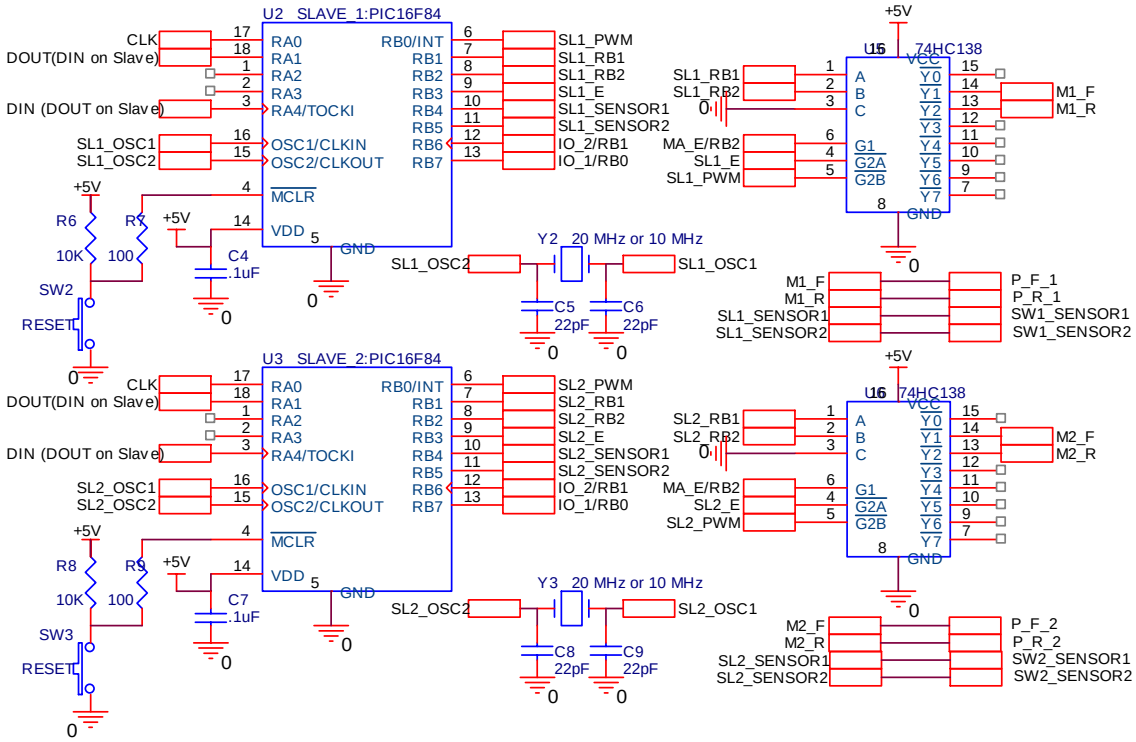

Figure 2: Multiple Slaves Hardware Circuit

2. Slave Control Circuit

The serial communication interface is implemented on PORTA where RA0 (CLK) is used to accept the clock signal from the master, RA1 (DOUT) is used to read the command bytes from the master, and RA4 (DIN) is used to send the ACK to the master. The PWM signal is generated from the TMR0 timer via interrupt control on RB0 pin [1],[3]. It is used to control the de-multiplexer output that eventually is used to regulate the energy to the DC motor. The PWM signal is generated constantly since it is an interrupt driven event. To gate this PWM to a proper channel (either forward or reverse control of the motor), RB3 (marked as SLX_E) is used as an enable control. Both RB1 (marked as SLX_RB1) and RB2 (marked as SLX_RB2) are used as channel select on the 74138 3-to-8 decoder that is functioning as a de-multiplexer [4]. The X on SLX stands for the number of the motor in the circuit.

There are two position sensors on each slave. The signals are monitored on RB4 (SLX_SENSOR1) and RB5 (SLX_SENSOR2) pins to provide feedbacks on the motor's position. The framing logic states are monitored on RB6 (IO_2) and RB7 (IO_1), which controls the slave's communication protocol sequences. There are two unused I/O pins, RA2 and RA3 on the slave circuit design. The multiple slaves are duplications of the following slaves' circuits that have two slaves as presented in Figure 2.

IV. The High Power DC Motors Controls

The motor driver circuit is a standard H-bridge design. These bridge on-off controls are made through an IRFB260N power MOSFET that can easily handle 10A-15A DC current [6]. The circuit can control a motor in either forward or reverse direction depending on the PWM signal that is coming in at its P_F_1 or P_R_1 terminal. Two position sensors have a RS latch debounce circuit to produce a clean feedback signal to the slave CPU. This motor circuit design is presented in Figure 3. Home Sensor (SWX_SENSOR1) and Ext Sensor (SWX_SENSOR2) are the position sensors that provide the positions of either full contract or extension. The X on SLX and SWX stands for the number of the motor in the circuit.

These I/O signals are connected to SLX_SENSOR1 and SLX_SENSOR1 pins of each slave processor module. Based on the digital logic of this DC motor control H-bridge design, the logic power (+5V DC) must be in place before the motor ($+V_{CC}$) to allow the gate to turn off the power to the MOSFET as a default state. Care must be taken on this required sequence, if the motor power ($+V_{CC}$) is supplied before the logic power, the power MOSFET will be turned on by the $+V_{CC}$ causing a direct short to the motor circuit.

The allowable combinations of motor controls are: (1) single motor running forward or backward, (2) two motors running forward or backward, (3) three motors running forward or backward, and (4) speed controls applied to all the motor combinations. The standard mounting of power MOSFETs soldered on a printed circuit board (PCB) with an attached head sink devices is not sufficient for this high current application. To accommodate the high current needs, the use of European terminal blocks on the PCB and the soldering of 14 gauge wires between the blocks and MOSFETs mounted on the heat sink is the necessary design solution.

The power supply made by Cherokee International, CAP1000 [7] providing 24 VDC, 50A max is used to supply power to all 10 different DC motors in this application.

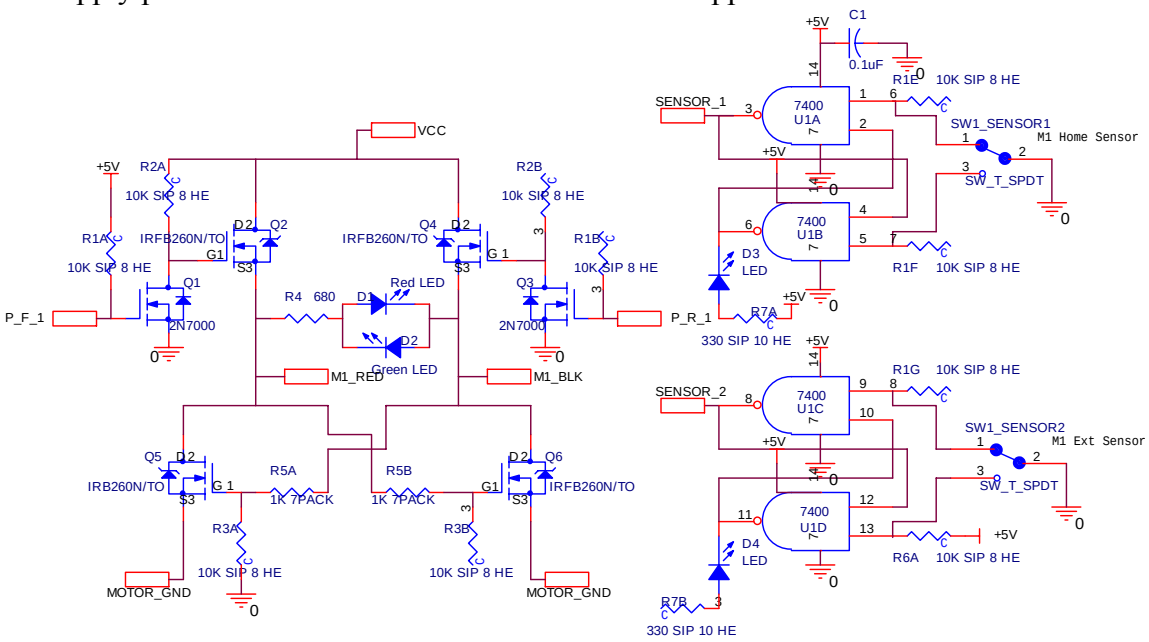

Figure 3: The DC Motor Control Circuits

V. The Communication Protocols

There are basically three I/O lines (clock (CLK), data in (DIN), and data out (DOUT)) dedicated for this communication [8]. These are all shared as a serial bus between a master and multiple slaves [8],[11],[12]. In each action of the serial communication bits streams, there are a total of five bytes, either transmit or receive, between a master and any particular slave CPU. The pre-defined bytes are: (1) address byte, (2) slave acknowledge byte, (3) speed byte, (4) direction byte, and (5) time period byte.

There are several sets of rules for this communication [9],[10],[12]: (1) only one master is allowed in the system, (2) only the master can generate the clock, (3) only the master can start/stop the communications, (4) only the master is responsible for the framing I/O bits, (5) there are multiple slaves allowed in the system, but each slave shall have a unique address recognizable by the master, (6) the slave can only monitor the framing I/O bit for communication responses, (7) the slave is required to respond to its address call by sending an ACK byte, (8) after the initiation of a start from the master, every slave has to read the address that master broadcasts, (9) the slave is not permitted to respond if its address is not called, and (10) the only time that the slave sends a byte is when it is required to ACK.

To ensure the safety of the system performance, an alarm condition is implemented in the event of violation of the protocol. The alarm condition is defined as: when the master sends a legitimate address to the slaves and does not receive an ACK or the ACK is not recognized for any reason. As soon as the master detects this alarm condition, it will disable the de-multiplexer that is used by the slaves to activate the motors.

At the beginning of the protocols testing stage, it was difficult to keep the master and slave synchronized. Therefore, the protocol rules mentioned above were introduced and framing I/Os were added. Two additional I/O pins were developed to frame the states of the communication bytes to correct the problem. They are the states that the master controls and slaves poll during each action. The framing I/Os are inputs to the slave. They are used to indicate to the slaves that the master is ready to do the next set of instruction. There are four different states (00, 01, 10, 11) the master sends to the slaves. Since the slaves don't perform as much work as the master, these states let the slaves recognize where the master is in the communication sequence. "00" informs the slaves as a start that the master is getting ready to send the first byte (address). Following the first byte, the master sends a "01" to notify the slaves it is ready to receive the ACK. When the I/O pins switch to "10", the slave knows that the master has received the ACK and is about to send the last three bytes. Finally, the master will send an "11" through the I/O pins, indicating it is done with the transmitting action.

The synchronous serial communication shares the same clock [9],[10],[11], and every party relies on the clock edges to either read or write the bits. The framing implementation resolves the timing issues and the differentiation of the start, end/stop, address, and command bytes. The presentation of the protocol bytes and associate framing I/O is presented in Figure 4. Figure 5 shows the real sample communication bits streams on clock (CLK), data out (DOUT), data in (DIN), and framing I/O (I_O1 & I_O2) lines that were captured by a logic analyzer.

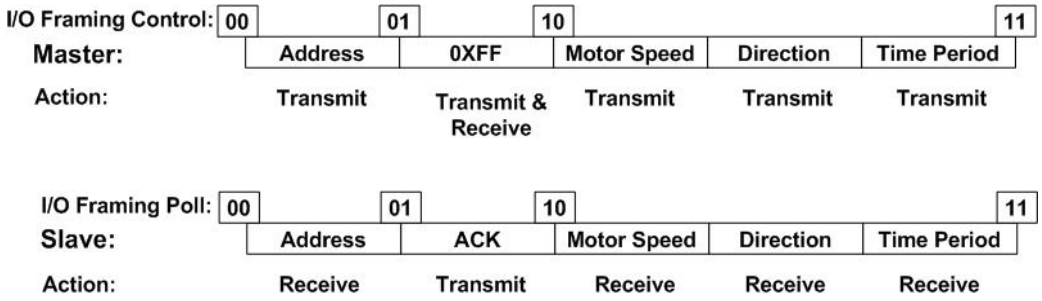

Figure 4: Master & Slave Protocols

VI. Tested Solutions to Noise Contaminations from DC Motors

The above circuits were tested with Pittman [9], GM92334C212-R3, 24VDC motors that running at 2.7A without any problem in controlling all the required sequences with various combinations. When the identical setup upgraded to high power, brush DC motor testing, there were severe noise contaminations that caused erratic behavior in the DC motors and an eventual short in the IRFB260N power MOSFETs. The contaminations were, at time, so bad that smoke was generated during first several tries to start the motors.

Different investigations were done to find the cause of these problems and solutions to minimize the noise contaminations. These tests included: (1) adding surge protection diode placed between the drain and source on every power MOSFET, (2) adding special 1µF protection capacitors between the power and ground lines in the processors and control logics, (3) adding 1 µF capacitors between the power and ground of all the serial communication signal lines, and (4) adding different combination of capacitors and inductor coils between the DC motor power terminals (MX_RED and MX_BLK). After numerous tests, the last method seems to have the most effects on reducing the noise contaminations.

Figure 5: The Sample of Serial Communication Signals

Table 1 shows the test results of different combination of capacitors and coils that added to the terminals on the DC motors.

Table 1: Capacitors and Coils Combination Test Results

Capacitor	**Coil**	**Time Delay between Motor Direction Change and Motor Activation**	**Note/Comment**
100 µF * 2	Small (0.14 µH, 1KHz)	Several seconds	This combination has little effect on noises.
220 µF * 2	Small (0.14 µH, 1KHz)	Several seconds	This combination has improvement on motor performance.
1000 µF * 2	Medium (0.35 µH, 1KHz)	One to Two Seconds	This is improved but needs long time delay.
2200 µF * 2	Medium (0.35 µH, 1KHz)	Above one second	Needs long time delay
4700 µF * 2	Medium (0.35 µH, 1KHz)	Around one second	Need long time delay
2200 µF & 6800 µF	Medium (0.35 µH, 1KHz)	Less than ½ second	This combination has the best improvement and acceptable time delay between motors performances.

Since the motors were controlled through the H Bridge that runs current in either direction on motors' terminals, the non-polarized capacitors are needed. The use of electrolytic capacitors' in a non-polarized condition requires connecting them back to back serially. That is one capacitor's – connected to the other's – terminal and the coil is placed on either side of the + terminal of these two capacitors. One side of the capacitor + and one side of the coil are then placed on to the motors' power terminals. In doing so, this will place the electrolytic capacitors in combination with a coil to accept either directions of the current flow and suppress the surges from the power supply and counter electric magnetic field (CEMF) effects from the motors' windings.

The starting current of a motor, on average, can get up to 5 - 6 times that of operating current. Running the brush motors under a constant changing of the motor direction and speed poses further difficulty. The current limit power resistors with a heat sink were added to the test circuit to reduce high starting current spikes. To compensate the performance of the motors, a 0.5Ω, 50W power resistor made by DALE [13] was connected in series with each motor current supply path. This modification improved the high current spikes with minimal reduction of motor performances.

The use of shield wire with added 1μF capacitors between +5V power and ground on all the position sensors circuit is also implemented to reduce the noise problem. Figure 6 presents the testing of hardware circuit boards and three high power DC motors.

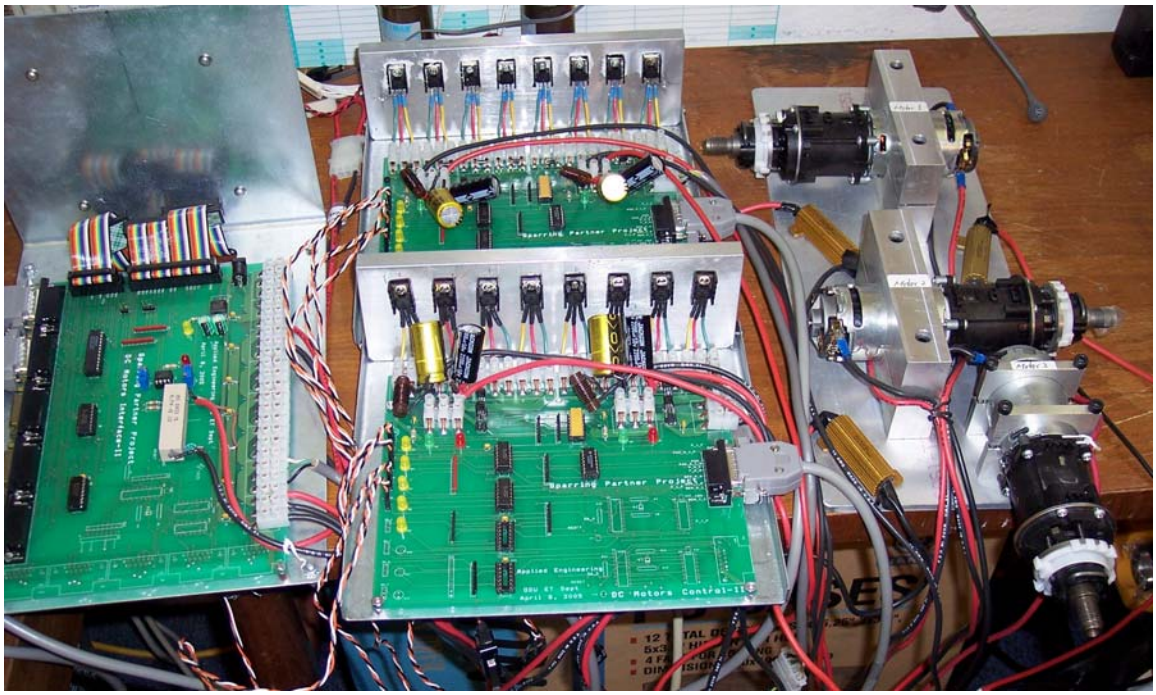

Figure 6: The Hardware Systems Test on Three Motors

VII. Conclusions

Engineering Technology is the application of science, technology, and mathematics. It is vital to the economic growth and success of the nation's future. Microprocessor/microcontroller

technology is a significant part of modern engineering and important subject matter in the Electrical and Mechanical Engineering Technology curricula.

Using multiple microprocessors/microcontrollers in automatic control applications is not new, but it is rarely implemented in classroom teaching environment. The process of designing application programs starts with individual module development and continues through extensive testing, verification, and modification. Applying these developed modules in a useful manner requires the links and integrations that lead to practical project implementation. Frequently, in students' senior project designs and faculty's research plans, the microprocessor/microcontroller resources become scarce, or cause conflicts during the modules' integration stage.

To accommodate the shortfall of the resources and resolve any conflict state, several choices must be considered, such as the need to revise or totally rework the module, or apply the module with additional circuit design. This article presents a proven concept that implements a simple serial communication protocols in a multi-processor environment, which aims to keep the pre-developed modules intact with the least possible modification when integrated into the project. The integration of the existing concept into a custom-made application brings real-life applications into classes, has served one of the important missions of the ET education: Applied Engineering.

All the designs work were done by the faculty involved in this project with students' assistance in testing and building of the module components. Those students (both electrical and mechanical majors) who involved in this project expressed great satisfaction in learning the microprocessor/ microcontroller control applications. When this project was in its testing stages and demonstrated to classes, it made a great difference in students' learning attitude and motivated them with unexpected interest in class material.

There are lessons learned in designing and developing of high power motors control circuits. The DC brush motor is a very noisy device and the CEMF during the start and reverse direction manipulations are particularly troublesome. First, it is very difficult to predict and measure the noise contamination level. Second, the noise changes along with different control pattern. Third, the locations of the noise contamination vary with the wiring, board layout, and location. All these variables make the implementation of the hardware and software designs difficult and they have to be tuned and modified stage by stage while linking the electrical and mechanical designs together. Table 1 presents the actual test data that fit in the actual performance criteria. Certainly, there are limits to this project and more research is needed in eliminating noise contamination. Using optical isolators between the motors and control processor circuits will be an area of continued research.

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IX. Biography

STEVE C. HSIUNG is an associate professor of Electrical Engineering Technology at Old Dominion University. Prior to his current position, Dr. Hsiung had worked for Maxim Integrated Products, Inc., Seagate Technology, Inc., and Lam Research Corp., all in Silicon Valley, CA. Dr. Hsiung also taught at Utah State University and California University of Pennsylvania. He earned his BS degree from National Kauhsiung Normal University in 1980, MS degrees from University of North Dakota in 1986 and Kansas State University in 1988, and PhD degree from Iowa State University in 1992.

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