A Low-power Technique for Extracting the Main Characteristics of an Analog Sine-wave Signal

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Abstract

In this paper, we propose a low-power integrated sine-wave analyzer for mixed-signal BIST applications. The analyzer extracts, in the digital domain, the DC level and the amplitude of the harmonics of a distorted analog sine-wave signal. This approach is based on a double modulation, square-wave, and ΣΔ, together with a simple digital processing algorithm. This is intended for the characterization of sine-wave signals in the range of audio. The required circuitry for on-chip implementation is simple and robust, which makes the present approach suitable for BIST applications. Solutions in this sense are addressed together with simulation results that validate the feasibility of the proposed approach.

I. Introduction

Testing of analog and mixed-signal circuits has become more and more difficult and created a bottleneck of the manufacturing process because the performance of these circuits is continuously increased. BIST (Built-In Self-Test) techniques can reduce the test costs, take the test paradigm to the design domain, and make the circuit auto-testable. To test digital parts, BIST techniques have been developed and widely implemented in current chips. In contrast, BIST techniques for analog circuits are not mature. Several strategies have been proposed for a structural BIST for modulators. An oscillation-based strategy was proposed in reference [1], where the modulator is reconfigured to be an oscillator. A digital BIST has been proposed for extraction of the integrator leakage and settling error in references [2] and [3]. Structural tests do not allow complete validation, so additional tests are necessary. The need for a stimulus with at least a precision of 3 bits greater than the converter under test [4] and the large digital resources needed for the analysis make the application of a functional BIST in high-resolution converters difficult. In reference [5], a binary stream generated by an on-chip-based digital oscillator was applied to the input of the converter. Usually, the test of the analog parts represents the main bottleneck in this line. Analog circuits are usually tested using functional approaches, often requiring large data volume processing, high accuracy, and high-speed ATE (automatic test equipment). In addition, these analog cores are normally sensitive to noise and loading effects, which limit the external monitoring and make their test a difficult task. Robust and efficient on-chip methods for the characterization

of sine-wave signals are of undoubted interest. They comprise the measurement of parameters such as frequency, amplitude, DC-level, distortion, signal-to-noise ratio, etc., and have a wide variety of potential applications in the field of analog and mixed-signal testing since most of these systems can be characterized by applying sinusoidal stimuli (filters, A/D and D/A converters, sigma-delta (ΣΔ) modulators, etc.). In addition, it is also a key point for the extension of the so-called oscillation-based test (OBT) [6, 7] to a full BIST scheme. The use of encoding schemes has been shown to be efficient for on-chip signal generation and evaluation. In reference [8], the generation of precise single and multi-tone sine waves was reported. On the other hand, the use of modulators as analog response extractors has proved useful [9]. The main advantages of these approaches are the simplicity and the robustness of the required circuitry, which make them very suitable for on-chip implementation and, hence, for BIST applications.

BIST schemes consist of moving part of the required test resources (test stimuli generation, response evaluation, test control circuitry, etc.) from the ATE to the chip [10]. BIST circuitry should have low area overhead, robustness against process variations and environmental noise, and properties of automation and reusability to reduce design efforts. This work aims to improve and extend the capability of the scheme proposed in reference [11] for the extraction of the amplitude, frequency, and DC level of the input signal, including the measurement of the harmonic distortion. A robust and area-efficient signal analyzer for BIST applications is thus obtained. This paper is organized as follows. In Section II, we will present a brief review of the sine-wave analyzer approach. Section III will show the internal structure for the integrated demonstrator. Section IV will describe the improved approach for the latch comparator with a clock generator and low-power comparator. Section V will present practical considerations for BIST applications. In Section VI, experimental results will be presented; and finally, in Section VII, the conclusions will be given.

II. Brief Review of the Sine-wave Analyzer Approach

Figure 1 [12] illustrates the block diagram of the modified approach for characterization of periodic signals and its timing diagram. In a switched-capacitor realization, the multiplication, which is needed, can be performed inside the modulator itself with proper switching.

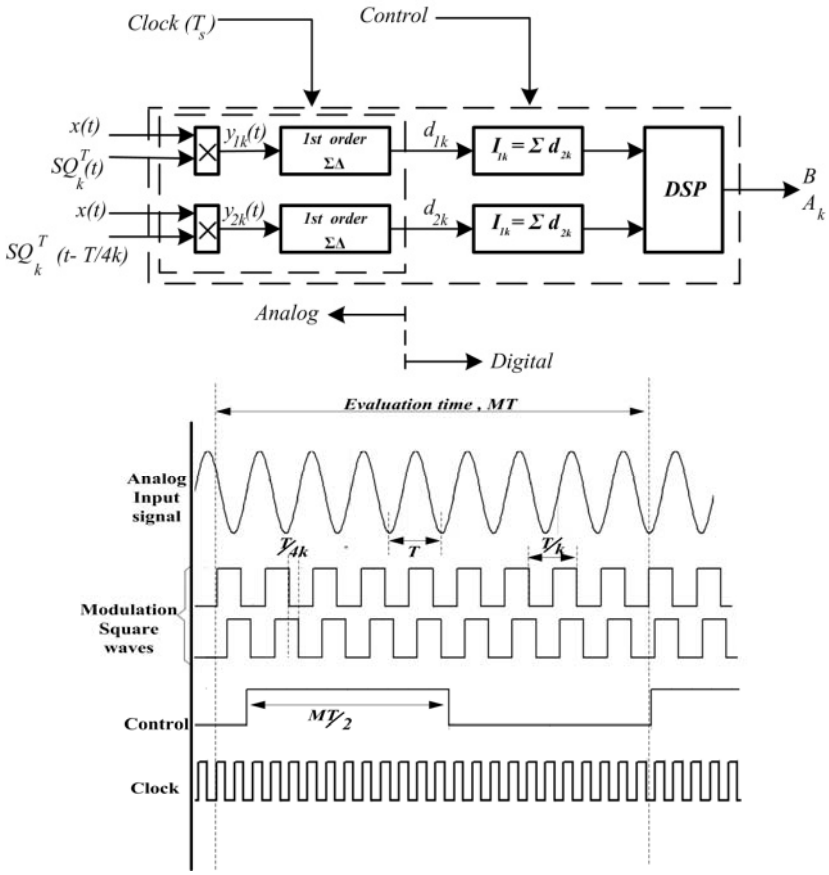

Figure 1: a) Block diagram of the approach for the characterization of periodic signals
b) Timing diagram [12]

Its functionality can be briefly described as follows. The signal under evaluation $x(t)$ is modulated by two square waves in quadrature, $SQ_k^T(t)$ and SQ_k^T $(t\text{-}T/4k)$, of amplitude 1 and period T/k, where T is the period of $x(t)$ and k is an integer. The resulting signals $y_{1k}(t)$ and $y_{2k}(t)$ are fed to two matched, first-order ΣΔ modulators. The generated bit-streams d_{1k} and d_{2k} are integrated along an integer number M of periods of the signal under evaluation using a set of counters to obtain the signatures I_{1k} *and* I_{2k}. These signatures are then processed using basic arithmetic operations in the digital domain (represented by the DSP block in Figure 1) to cancel the offset contribution of the modulators and to obtain the main parameters of $x(t)$: DC level, amplitude of the harmonic components, and their corresponding phase shifts. Namely, if M is even and $N/23k$ is an integer number, where N is the oversampling ratio in the modulator defined as $N=T/Ts$ (where Ts is the sampling period), the DC level (B) and the amplitude of the k-th harmonic (A_k) can be ensured to be confined in bounded intervals given by [12],

$$B \in \frac{1}{MN}[I_{10} - \varepsilon_{10}, I_{10} + \varepsilon_{10}] \quad or \quad \frac{1}{MN}[I_{20} - \varepsilon_{20}, I_{20} + \varepsilon_{20}]$$

$$(A_k)^2 \in \left(\frac{\pi}{2}\frac{1}{MN}\right)^2 \begin{bmatrix} \min\{(I_{1k} + \varepsilon_{1k})^2 + (I_{2k} + \varepsilon_{2k})^2\}, \\ \max\{(I_{1k} + \varepsilon_{1k})^2 + (I_{2k} + \varepsilon_{2k})^2\} \end{bmatrix} \tag{1}$$

where $\varepsilon_{1k}, \varepsilon_{2k}$ (k= *0, 1, 2...*) are unknown error terms (due to the quantization noise in the modulator) but limited to $\varepsilon_{1k}, \varepsilon_{2k} \in [-4, 4]$. Thus, the relative errors of the measurements can be reduced by increasing the total number of samples (*MN*). This analyzer approach has different attributes that make it interesting for BIST applications.

On one hand, the required analog circuitry is limited to first-order modulators, while its simplicity and robustness is well known. On the other hand, the majority of the signal processing is made in the digital domain. This opens the possibility to integrate it on-chip or be realized externally with a digital ATE.

The response of a first-order modulator can be expressed in terms of its input signal *y* and the quantization error *e* as:

$$d(n) = y(n-1) + e(n) - e(n-1) \tag{2}$$

The sum of the bit-stream along a number *q* of samples is then given by:

$$\sum_{n=1}^{q} d(n) = \sum_{n=0}^{q-1} y(n) + \{e(q) - e(0)\} \tag{3}$$

Signal *x(t)* has harmonic components. It can be described in terms of its Fourier series expansion in the form:

$$x(t) = B + \sum_{k=1}^{4} A_k \sin(k\omega t + \phi_k), \tag{4}$$

where A_k and k represent the amplitude of the k-th harmonic component and its corresponding phase shift, respectively.

If the ratio of the sampling frequency to the input signal frequency *N=fs/f=T/Ts* in the modulator is high enough, the discrete summation of $y(n)$ approaches the continuous time integration of $y(t)$. Therefore, if the sum is extended to an integer number of periods *M* of *x(t)*, the result will be practically the same except for a quantization error term. In fact, it can be shown that the error due to sampling can be neglected with respect to the quantization error. In this way, simple digital counters, as in reference [11], process the bit-streams at the output of each modulator. The possibility of realizing the measurement sequentially is discussed in Section V. Two measures, I_{1k} and I_{2k}, are thus obtained for the two square waves in quadrature $SQ_k{}^{T}(t)$ and $SQ_k{}^{Td}(t)$.

Table 1 gives the expected counter values for each harmonic k as a function of the oversampling ratio *N*, the number of averaging periods *M*, and the input signal parameters (B,A_k and φ_k, k=1,2,3,4). As $[(\sin x)^2+(\cos x)^2]=1$, it should be clear that each frequency component of *x(t)* can be estimated by computing $[(I_{1k})^2+(I_{2k})^2]$.

In the case of A_1, it appears with A_3 ($k=1$). However, if $A_1 >> A_3$ as is usual, the contribution of A_3 in $k=1$ can be neglected (this is even more true if the summation is extended to a small number of periods). Otherwise, the contribution of A_3 can be subtracted as it is extracted when $k=3$.

Table 1: Results at the output of the counters. (M=number of periods, N=oversampling ratio, $|\varepsilon|$, $|\varepsilon_d| \in [-2,2]$)

k	R_k	R_{kd}
0	$B(MN) + \varepsilon$	$B(MN) + \varepsilon$
1	$MN(2/\pi)[A_1 cos\varphi_1 + (A_3/3)cos\varphi_3] + \varepsilon$	$MN(2/\pi)[A_1 sin\varphi_1 + (A_3/3)sin\varphi_3] + \varepsilon_d$
2	$MN(2/\pi)[A_2 cos\varphi_2] + \varepsilon$	$MN(2/\pi)[A_2 sin\varphi_2] + \varepsilon$
3	$MN(2/\pi)[A_3 cos\varphi_3] + \varepsilon$	$MN(2/\pi)[A_3 sin\varphi_3] + \varepsilon$
4	$MN(2/\pi)[A_4 cos\varphi_4] + \varepsilon$	$MN(2/\pi)[A_4 sin\varphi_4] + \varepsilon$

III. The Internal Structure

This section is dedicated to presenting the design of the integrated demonstrator. Although only the analog part has been integrated (it includes the first-order modulator and the square wave modulation), some considerations for the digital part will also be given.

1. ΣΔ and square-wave modulator

A block diagram of a first-order ΣΔ modulator is shown in Figure 2 [13]. The system consists of an analog ΣΔ modulator, followed by a digital decimator. The modulator consists of an integrator and a D/A converter (DAC) used in the feedback path.

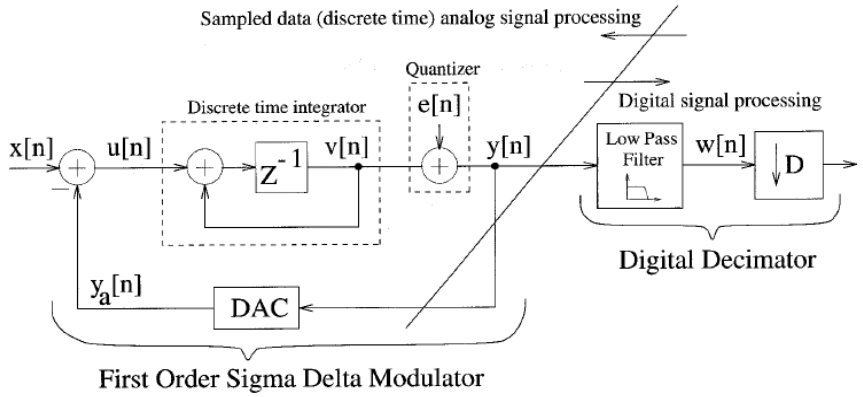

Figure 2: First-order ΣΔ modulator

The quantizer is replaced by simple additive white noise as in Figure 2, which is a linearly simple, but true, model of quantization noise. The transfer functions from the quantization noise (N_q) and the input signal to the output are as follows:

$$STF = \frac{Y}{X} = \frac{H(Z)}{1+\beta(Z)H(Z)} \tag{5}$$

$$NTF = \frac{Y}{N_q} = \frac{1}{1+\beta(Z)H(Z)} \tag{6}$$

$$Y(z) = STF(z)X(z) + NTF(z)E(z), \tag{7}$$

where $X(z)$ and $E(z)$ are the Z-transform of the input signal and quantization noise. $H(z)$ and $\beta(z)$ are the transfer functions from the discrete time integrator and the DAC, respectively; and $STF(z)$ and $NTF(z)$ are the respective transfer functions of the input and quantization noise. In this paper, we will focus on the one-bit-quantizer modulator only.

Figure 2 shows the conventional first-order modulator with the linear quantizer model, where $H(z) = 1/1- z^{-1}$. The signal transfer function (STF) is unity, STF=1, while the NTF is given by NTF=1- z^{-1}. Assuming that the quantization error is largely uncorrelated from sample to sample and has statistical properties, which are independent of the signal, the SNR can be calculated as [14]

$$SNR = 10\log_{10}(\sigma_{xy}{}^2) - 10\log_{10}(\sigma_{ey}{}^2) - 10\log_{10}(\frac{\pi^2}{3}) + 9.03r(dB), \tag{8}$$

where σ^2_{xy} is the variance or the signal power at the output, and σ^2_{ey} is the variance or the in-band noise power at the output-assuming zero mean. Since the signal power is assumed to occur over the signal band only, the signal power is not modified in any way, and the signal power at the output σ^2_{xy} is the same as the input signal power σ^2_x . The sampling frequency is given by f_s and the input signal bandwidth is given by f_B ; r is given by (OSR) where OSR is defined as OSR = (f_S / $2f_B$) = 2^r. For every doubling of the OSR, for every increment in r, he SNR improves by around 9 dB.

The discussion has so far neglected stability issues. Modulators of order (L > 2) are only conditionally stable [15]. Stabilizing a higher-order loop requires the use of more complicated transfer functions than just a cascade of integrators in the forward path of the modulator and possibly the use of circuits that reset the state variables in the integrators when instability is detected. Unfortunately, the methods required to stabilize a higher-order loop reduce the modulator DR.

Figure 3 [12] shows the schematic of a fully differential first-order ΣΔ modulator where the switching input interface has been properly modified for this application. It operates with two non-overlapping clock phases (ϕ_1 and ϕ_2) and a digital control signal q_k. It is easy to show that, depending on the logic value of q_k (high or low), the weight of the sampled input (V_{in}) is

positive or negative. This switching scheme has been used to perform the required square-wave modulation in the ΣΔ modulator itself.

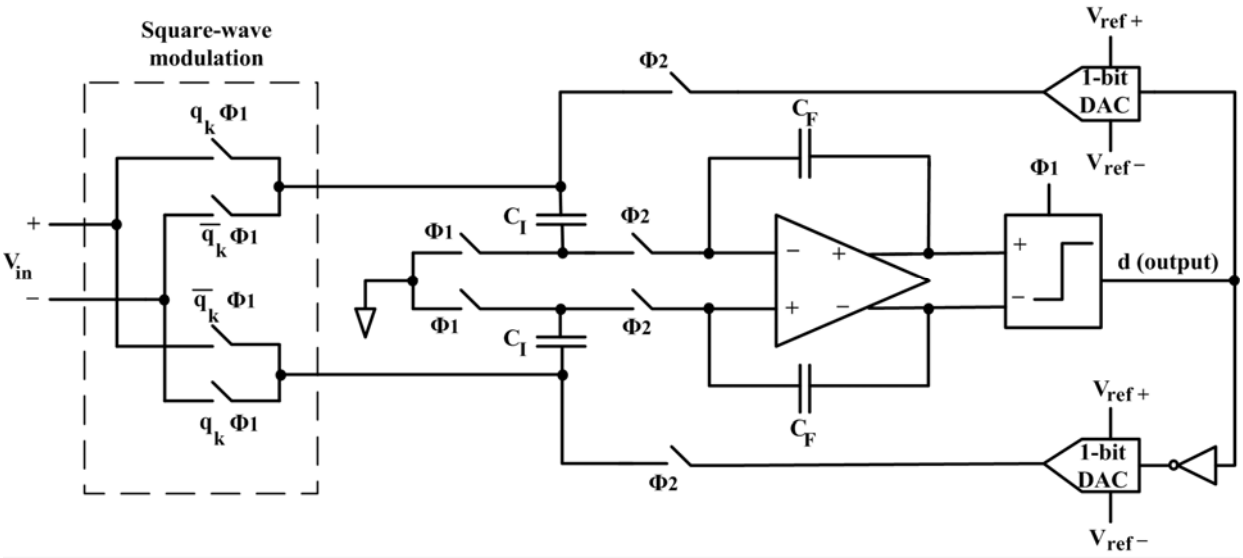

Figure 3: ΣΔ modulator with square-wave input modulation [12]

2. The amplifier

The amplifier is the most critical block in the modulator. Its characteristics in terms of DC gain, bandwidth, slew rate, settling time, etc., define the performance of the modulator. The folded-cascode architecture in Figure 4 has been chosen. The architecture offers very high output impedance, moderate gain, and high bandwidth. Table 2 lists the size of the transistors. The dynamic circuit in Figure 4 provides the common mode feedback. The 1.2-pF capacitor connected to the output node provides the necessary frequency compensation for the amplifier.

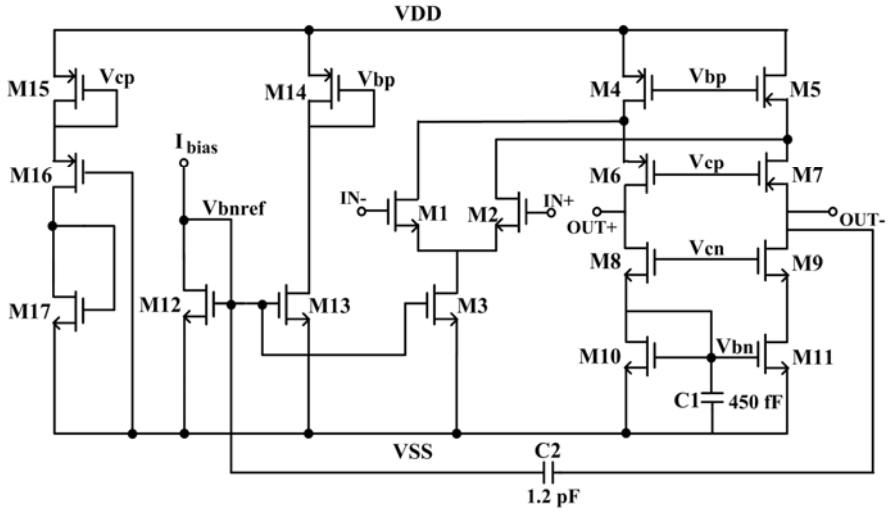

Figure 4: Fully differential folded-cascode amplifier

Table 2: Transistor sizes in the amplifier (0.35-µm technology)

	M1=M2	M3	M4=M5	M6=M7	M8=M9
W (µm)	100	96	180	180	96
L (µm)	1	1	2	1	1
	M10=M11	M12=M13	M14	M15=M16	M17
W (µm)	48	16	30	5	2.6
L (µm)	1	1	2	4	4

IV. Improved Approach for Latch Comparator with Clock Generator and Low-power Comparator

The main problem of a low-voltage comparator is to do the rest. A ΣΔ modulator does not need a comparator with high resolution, but requires low hysteresis, so a good reset is important. This section describes an approach to improve the comparator, latch part, and clock generator for completing this modulator. Figure 5 shows the schematic of a low-power comparator, which is suitable for the modulator under consideration. This comparator may be operated with a low (1 µA) bias current, since the speed requirements are quite lax and the modulator is tolerant of comparator offset. Simulations indicate that the power consumption of this circuit is less than 3.85 µW at a clock frequency of 5 MHz, so the power consumed by the quantizer will be a very small portion of our budget. Figure 6 shows the schematic of a common latch, while Figure 7 depicts a widely used clock generator.

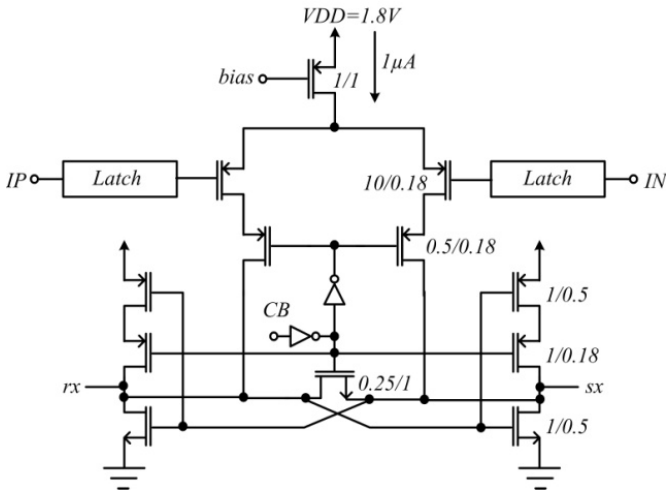

Figure 5: A low-power comparator

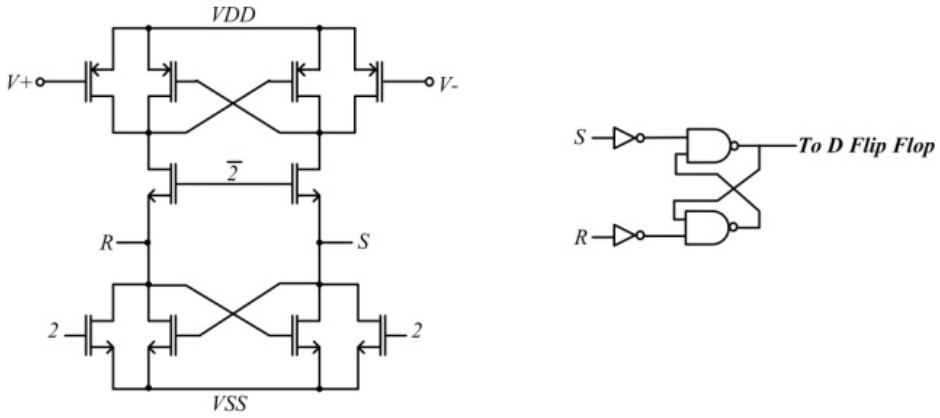

Figure 6: Latched comparator

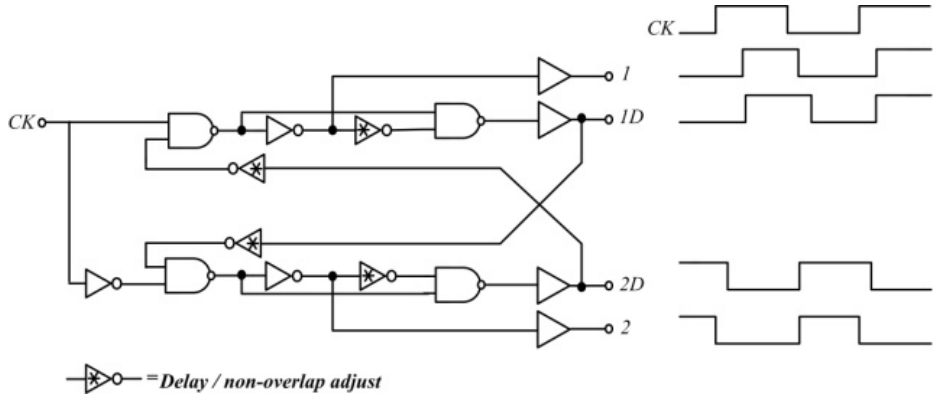

Figure 7: Non-overlapping clock generator

V. Practical Considerations for BIST Applications

As mentioned in Section II, the work in reference [11] proposed to realize the multiplication by a square wave in the digital domain, at the output of the modulator. In fact, this could still be applied here, and all the I_{1k} and I_{2k} measurements could be realized in parallel at the expense of one counter in the DSP processor per parameter. However, the back-end multiplication leads to a loss of accuracy due to the incomplete cancellation of the quantization error in the modulator. For the same accuracy, the required number of samples would be much higher for the backend than for the front-end multiplication. Hence, the measurement of small harmonics would require a prohibitive number of samples for the back-end modulation.

In a switched-capacitor realization, the front-end multiplication can be performed inside the modulator with proper switching. Nevertheless, a price has to be paid for this multiplication. The measurements can no longer be realized in parallel, unless more than one modulator is implemented. As can be seen in Figure 1, two matched modulators are used to calculate I_{1k} and I_{2k} in parallel, but it would be possible to realize the measurements sequentially.

Actually, a trade-off exists between the test-time and the area. If the measurements are realized sequentially, only one modulator and one counter are required, plus some memory to store each I_{1k} and I_{2k} value. If the measurements are realized fully in parallel, a modulator and a counter are required for each I_{1k} or I_{2k}.

VI. Experimental Results

To examine the performance of the proposed modulator and low-power comparator architecture, they are simulated in MATLAB and HSPICE. The waveforms in Figure 8 show a dramatic illustration of the (apparently) poor correspondence between the input of a ΣΔ modulator and its output. As this figure shows, the only similarity between the input and output waveforms in the time domain is that when the input is positive, the output is usually either +2 or 0, and when the input is negative, the output is usually either –2 or 0.

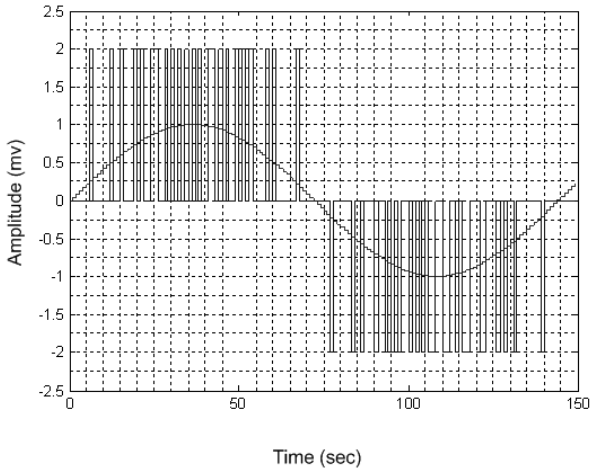

Figure 8: MATLAB code for simulating a ΣΔ modulator and for plotting a portion of the output waveform

As shown in Figure 4, a modified op-amp is used in the modulator but with the NMOS input stage, instead of PMOS, to achieve higher gain bandwidth. Fully differential flooded-cascode is used in the amplifier to bias the input differential pair in the saturation region for a 3.3V supply voltage. Cascade transistors are added to the output stage to achieve the required DC gain, not to degrade seriously the *SNR* and DR of the modulator. V_{bp}, V_{cp}, and V_{cn} are the bias voltage. The amplifier specifications are in Table 3. These specifications are more than enough for the intended application.

The proposed comparator in this paper has been simulated in a 0.35-μm standard CMOS technology. This comparator is used in this paper because the power supply voltage of the comparator is only 1.8 V and operates with a low (1 μA) bias current, and the output of the comparator drives a high-speed current switched feedback DAC. These specifications are

important when using this type of comparator. Table 4 shows the performance characteristics of the comparator.

Figure 9 shows the simulation results of the square-wave modulation output. Figure 10 shows the simulation results of the output of the amplifier.

Table 3: Amplifier performance (Add=3.3 V, Ibias=60 μA)

Parameter	Value
DC gain	41 dB
GBW	258 MHz
S.R	126 V/μSec

Table 4: Comparator performance

Parameter	Value
VDD	1.8 V
I_{bias}	1 μA
V_{OH}	VDD – 0.6 V
V_{OL}	0.3 V
I_{SRC}	67.81 μA
t_p	0.2 μSec
P_{max}	3.85 μW

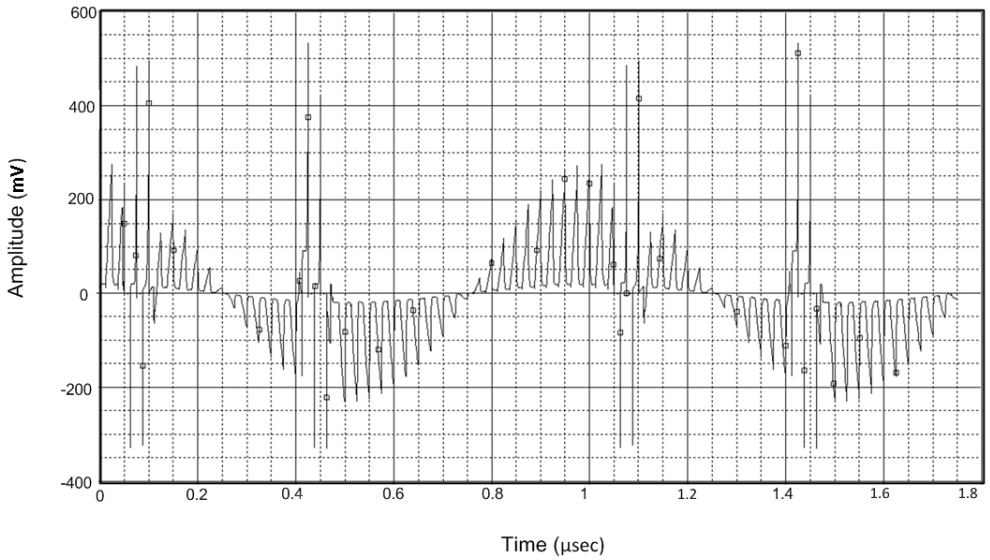

Figure 9: The square-wave modulation output

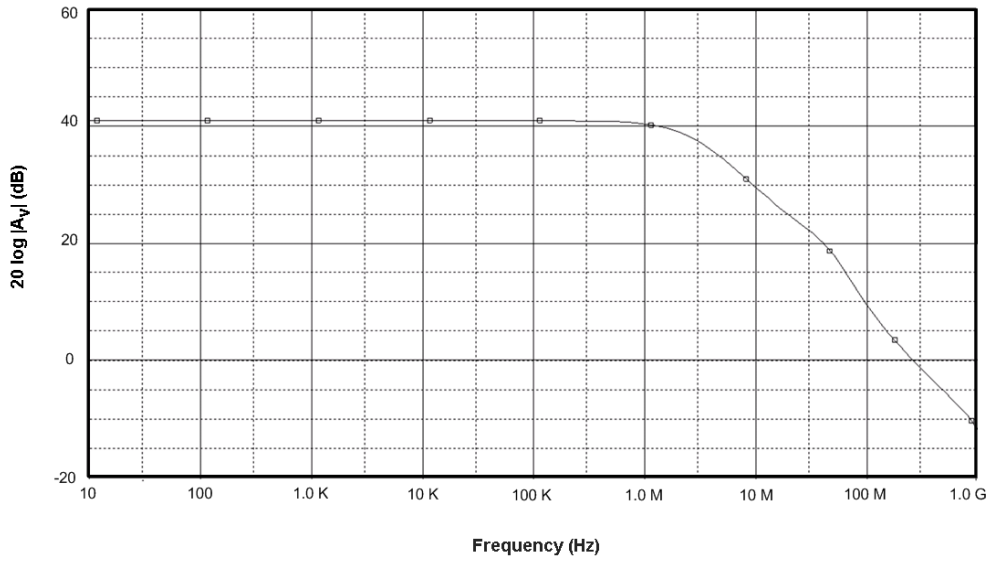

Figure 10: Bode diagram of the amplifier

VII. Conclusion

This paper has presented an approach for the characterization of sine-wave signals using a first-order ΣΔ modulator. It is able to characterize distorted sine-wave signals by extracting the DC level and the amplitude of the harmonics that compose the signal in the digital domain. The required circuitry for the implementation of the approach consists of a first-order modulator, low-power comparator, low-power latch, and a simple digital logic. It is simple and robust and makes the present approach suitable for on-chip implementation. In addition, the main processing of the data is performed in the digital domain through basic arithmetic operations. Moreover, in a switched capacitor realization, the modulation of the input signal $x(t)$ can be performed inside the modulator through the proper control of the switches and capacitors. The simplicity and robustness of the circuitry make it suitable for BIST applications.

Acknowledgement

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References

[1] G. Huertas, D. Vázquez, E. J. Peralías, A. Rueda, and J.L. Huertas, "Oscillation-based Test in Oversampling ΣΔ Modulators," *Microelectronics Journal*, Vol. 33, 2002, pp. 799–806.

[2] G. Leger and A. Rueda, "Digital Test for the Extraction of Integrator Leakage in 1st- and 2nd-order ΣΔ Modulators," *IEE Proceedings on Circuits, Devices and Systems*, Vol. 151, no. 4, Aug. 2004, pp. 349–358.

[3] G. Leger and A. Rueda, "A Digital BIST for Amplifier Parametric Faults in ΣΔ Modulators," Proceedings of the IEEE International Mixed-Signal Testing Workshop, Cannes, France, June 2005, pp. 22–28.

[4] K. Parthasarathy, T. Kuyel, D. Price, L. Jin, D. Chen, and R. Geiger, "BIST and Production Testing of ADCs Using Imprecise Stimulus," *ACM Transactions on Design Automation of Electronic Systems*, Vol. 8, no. 4, Oct. 2003, pp. 522–545.

[5] M.F. Toner and G.W. Roberts, "A BIST Scheme for an SNR Test of a Sigma-Delta ADC," Proceedings of the IEEE International Test Conference, Baltimore, USA, Oct. 1993, pp. 805–814.

[6] K. Arabi and B. Kaminska, "Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, no. 7, July 1997, pp. 745–753.

[7] G. Huertas, D. Vázquez, E. J. Peralías, A. Rueda, and J. L. Huertas, "Practical Oscillation-based Test of Integrated Filters," *IEEE Design & Test of Computers*, Vol. 19, no. 6, 2002, pp. 64–72.

[8] B. Dufort and G. W. Roberts, "On-Chip Analog Signal Generation for Mixed-Signal Built-in Self-Test," *IEEE Journal of Solid-State Circuits*, Vol. 33, no. 3, March 1990, pp. 318–330.

[9] H. C. Hong, J. L. Huang, K. T. Cheng, C. W. Wu, and D. M. Kwai, "Practical Considerations in Applying ΣΔ Modulation-Based Analog BIST to Sampled-Data Systems," *IEEE Trans. on Circuits and Systems-II*, Vol. 50, no. 9, September 2003, pp. 553–566.

[10] SIA Roadmap for semiconductors. http://public.itrs.net.

[11] D. Vazquez, G. Huertas, G. Leger, E. Peralias, A. Rueda, and J. L. Huertas, "On-chip Evaluation of Oscillation Based Test Output Signals for Switched-capacitor Circuits," *International Journal of Analog Integrated Circuits and Signal Processing*, Vol. 33, 2002, pp. 201–211.

[12] D. Vázquez, G. Huertas, A. Luque, M. J. Barragán, G. Leger, A. Rueda, and J. L. Huertas, "Sine-wave Signal Characterization Using Square-wave and Sigma-delta Modulation," *Journal of Electronic Testing: Theory and Applications*, Vol. 21, 2005, pp. 221–232.

[13] J. Candy, "A Use of Double Integration in Sigma-Delta Modulation," *IEEE Transaction on Communications*, Vol. 33 August 1988, pp. 972–979.

[14] R. Schreier and G. Temes, "Delta-Sigma Data Converters: Theory, Design, and Simulation," S. Norsworthy, Ed. New York: IEEE Press, 1997.

[15] J. Candy and G. Temes, "Oversampling Methods for A/D and D/A Conversion," in Oversampling Delta-Sigma Data Converters. New York: IEEE Press, 1992.

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