Development of a Compact Three-Phase Induction Motor Drive System with Discrete Components

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Abstract

Growth in the high volume market in variable speed drives (VSDs) is expected due to emerging applications in home appliances, heating, ventilating, and air conditioning (HVAC) drives, professional hand tools, automobile accessories, fans, pumps, and process drives. VSDs greatly improve efficiency in those applications. Almost all of these applications do not require precise positioning or speed control and, hence, are of low performance types. They are very cost-sensitive as the make or break decision about their introduction is primarily decided by the cost only in spite of their advantages. Some of them are energy savings and control and operational flexibilities. The inverter-controlled induction motor drive (IMD) is a strong competitor for such applications due to the low-cost of the motor and to its inherent features, such as the simplicity of control requiring no sensors in these low performance applications. It is brushless, as it has no slip rings, thus making it truly almost maintenance-free and robust. This paper addresses issues of design and development of such a low-cost inverter and its controller to obtain one horsepower variable speed IMD. In addition, an implementation of VSD with analog and discrete components is discussed thoroughly. The various issues addressed in detail are: specifications, appropriate control strategy and drive configuration, design of control circuits, and their switching and conduction losses and tuning. Results from a fully tested one-horsepower experimental inverter controlled induction motor drive system are presented to correlate the key design aspects and design specifications. The proposed VSD for the three-phase induction motor is implemented mostly with analog and discrete components; it will be very useful to students in electric motor drive course to get an insight of a three-phase inverter and hands-on experiences to build and test a system.

1. Introduction

Emerging high volume VSD applications have the stringent requirements of low-cost and compact packaging for the electronic inverter and its controller to induce the conversion of many fixed speed applications to VSD operations with very little added cost due to the extra electronic components. The presentation of various studies would enhance the design and development concepts leading to the achievement of low-cost and compact drives for the motor drives market. Such a study of the design and development of a one-horsepower inverter and its controller for an IMD achieving the specified requirements is presented in this paper. Furthermore, the proposed VSD for the three-phase induction motor is implemented mostly with analog and digital discrete components to gain insight into a three-

phase inverter system and hands-on experience in building and testing a VSD for electric motor drives course.
The induction motor is essentially a constant speed machine if a constant voltage and frequency source is connected [1]. When the load torque increases, the induction motor speed drop will be minimal, which is the advantage for the constant speed applications. Many single chip microprocessor or digital signal controller (DSC) solutions to design a three-phase inverter for induction motor based VSD involve software design heavily; thus they are not suitable solutions for this study [2, 3]. However, the software control of VSD is desirable for providing flexibility of control and tuning without tinkering with hardware components, but it may not be sufficient to deal with details of VSD system implementation without a background in specific software language programming skills. The exposure of the major functional subsystems of the VSD to students is very important to the understanding of the overall system requirements and the design circuitry to meet the system requirements. The design philosophy in this study is to use as many commercial-off the shelf (COTS) discrete analog and digital components as possible to provide rich insight into the IMD system and plenty of hands-on opportunities for the students to understand, analyze, and build it [3-15].

The highlights of this study are as follows: The specifications of the drive system and the rationale for choosing a drive system control strategy are explained first. Then the subsystems of the proposed IMD are functionally identified. The design concepts of various subsystems and their implementation are explained. The outlines of the drive losses which lead to the selection of cooling arrangement satisfying the cost and packaging requirements are explained. The layout and final assembly of the power and control circuits are described along with the packaging details including that of the enclosure. Experimental results from the prototype inverter-fed IMD are presented to validate the design and conformity to specifications. As a conclusion, various teaching topics for electric motor drives course are suggested, based on the proposed IMD system.

2. Drive System Specifications and Selection of a Control Strategy

2.1 System Specifications

The induction motor considered for the development of the inverter and its controller is one-horsepower with three-phase windings and two poles, even though the number of poles does not affect the general design and development approach outlined in this paper. The ac input available is single-phase either with 50 or 60 Hz and 240 V. The design is modifiable for 120 V ac input, hence the power rating of the inverter, without any modification, may be considered for 0.5 hp.

The following general requirements and desirable features are the starting points for consideration of a IMD system design strategy: first quadrant operation capability which means motoring operation only, variable stator voltage and variable stator frequency (VVVF), variable voltage with pulse-width modulation (PWM) at a low-frequency to enhance efficiency of the overall IMD system, soft starting, current-limiting feature for the protection of the inverter, variable PI speed controller gains, and provision for operation with and without tachogenerator feedback. In addition to the above mentioned requirements, the

following specifications summarized in Table 1 are considered satisfactory most for fan/pump types of loads.

Table 1. Target Specifications of the Proposed IMD

Power Source	Single-Phase, 240 V ac, 50/60 Hz
Output Power	1 hp maximum, three-phase
Output Voltage Range	0 to 220 V rms (line-to-line)
Output Frequency Range	0.1 to 86 Hz
Commanded Speed Reference Voltage	5 V for the rated speed
Measured Speed Input Voltage	50 V maximum at rated speed
Modulation Method	Sine-triangular PWM (SPWM)
Carrier Frequency	2.78 kHz
Protection Features	Current and torque limitation with undervoltage operation prevention
Adjustments	Soft start controller time constant, proportional and integral speed controller gains, torque limit, offset voltage, V/Hz ratio, and dc bus current limit
Ambient Temperature	0 to 40 ^{o}C (70 ^{o}C with derated output power)
Cooling Method	Forced air cooling
Target Package Volume	100 cubic inches

The parameters of the single-phase equivalent circuit of an induction motor are obtained by these measurements [1]: After running the motor for a while until it get warmed up, the stator resistance, R_s is determined from three dc resistance measurements between each pair of motor phases, and the obtained data were averaged and divided by two. Other measurements are undertaken with the no-load test at the synchronous speed (3,600 r/min) and the locked rotor test at zero speed. The induction motor ratings and measured and calculated parameters are listed in Table 2.

Table 2. Induction Motor Ratings and Measured Parameters

Ratings of the Induction Motor under Test	1 hp, 230 V, 3 phase, 60 Hz, 3 A, 3450 r/min, 2 pole, Y-connected
Measured and Calculated Induction Motor Parameters at 60 Hz	R_s=2.355 Ω, R_r=2.055 Ω, L_m=183.4 mH, L_{ls}=L_{lr}=7.388 mH

2.2 Selection of Drive Control Strategy

Based on the drive specifications, the most important first step is to identify the appropriate control strategy for the inverter-fed induction motor drive. The volts-per-hertz (V/Hz) control strategy is selected because it has sufficient performance from the point of view that it requires simple control circuitry [1]. It keeps the flux magnitude in the motor approximately

constant by maintaining the voltage-to-frequency ratio constant except for a small resistive voltage offset. It is also not dependent on feedback signals for open-loop operation, requires very simple tuning in the form of its offset trimming and the change of voltage-to-frequency ratio. As the frequency becomes small at low speed, the voltage drop across the stator resistance can no longer be neglected; thus, an offset or boost voltage is necessary to provide the rated flux at low speeds. The effect of the offset voltage is negligible at higher frequencies. That even stator current measurement and feedback are not essential to this strategy is an important factor to be noted. All other control strategies, such as vector control, constant airgap flux control, and slip control, involve a greater use of control circuitry and feedback sensors, though they offer much more precise control of torque and speed. Since these control strategies involve rigorous code development efforts with a microprocessor or DSC, they are therefore not considered in this study in order to implement a simple controller with discrete analog and digital components.

3. Overall Drive System

The simplified block diagram of the proposed IMD incorporating the V/Hz control strategy is shown in Figure 1. The speed reference, ω_m^*, is processed through a soft start circuit whose time constant can be adjusted externally with a potentiometer. The output of the soft start circuit provides the modified speed command from which the filtered speed feedback signal is subtracted to provide the speed error. The speed error is amplified and processed through a proportional- plus- integral (PI) controller resulting in the torque command, T^*, which is further processed through a torque limiter. The torque limiter constrains the torque to be within the stable region of the steady-state torque slip region and, in the process, also limits the currents to be within the permitted levels.

In the stable operating region the torque is proportional to the slip speed; hence, the output of the torque limiter could be taken as slip speed command, s^*. The slip speed command is added to the filtered normalized rotor speed, obtaining the normalized stator angular speed command or normalized stator frequency command, f_n^*. The stator frequency is multiplied by the voltage-to-frequency ratio and added to the stator offset voltage, V_o, to provide the stator voltage command. The offset voltage is intended to overcome the reduction of the airgap voltage and, hence, in the weakening of the magnetizing current due to the large stator resistive voltage drop at low speeds. The stator frequency and voltage commands are then fed to a sine wave generator block to generate the three-phase stator voltage commands. These phase voltage commands are translated to actual phase voltages through SPWM with a triangular carrier frequency and obtaining a set of gate drive signals to the inverter bridge. The dc input voltage to the inverter is obtained through a diode full-bridge rectifier fed from a single-phase ac supply. It can be any dc voltage sources, such as a solar panel and a wind generator with or without a front-end boost converter to control the dc bus voltage level.

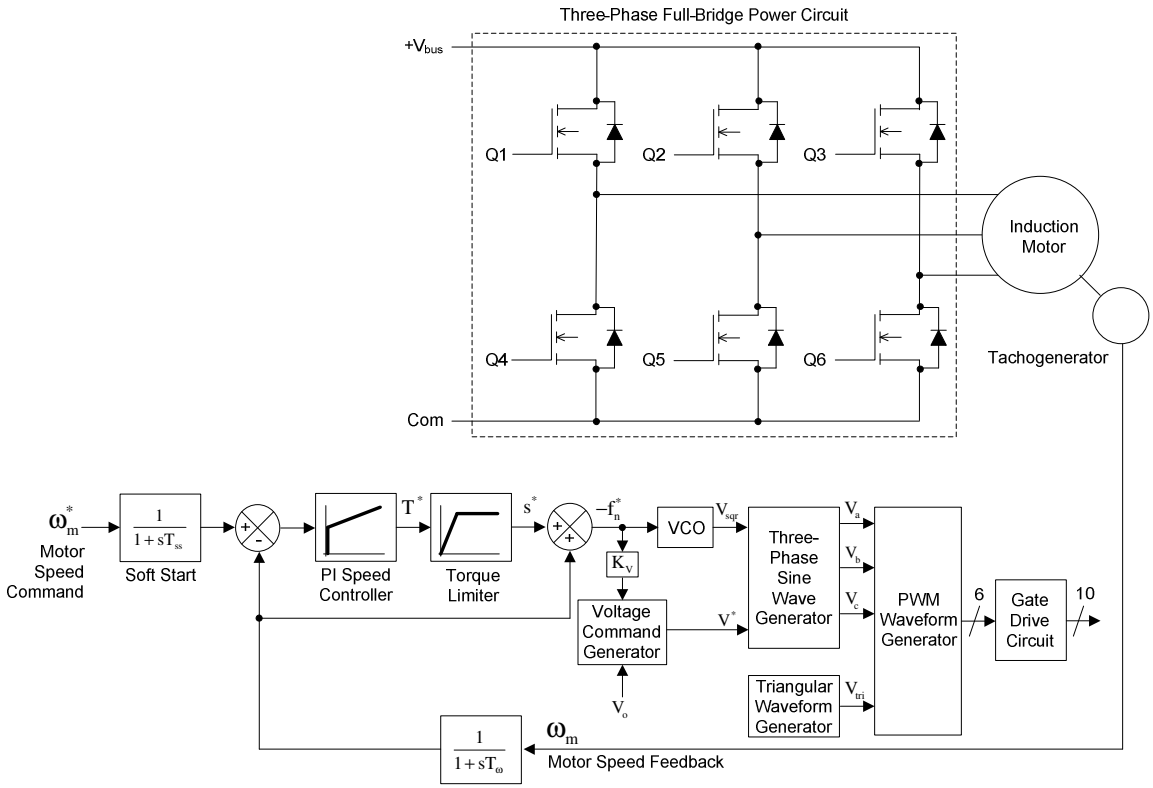


Figure 1. Block diagram of the proposed IMD incorporating the constant V/Hz technique.

4. Drive System Design and Realization

4.1 Design of IMD System

The various major subsystems shown in Figure 1 are considered for design and implementation in this section. The schematic of each block and the realization with discrete analog and digital components may lead to an application specific integrated circuit (ASIC) packaging if this design is to be adopted for manufacturing. But at this stage of prototype verification, it was decided to avoid the cost associated with such a development. Furthermore, the implementation of such a drive system with a microprocessor is not an option in this study to provide an insight of the drive system which consists of discrete components only. Either a microprocessor (microcontroller) or DSC solution to implement a drive system usually involves significant software development effort.

For the PWM signal generation in this study, the sine-triangular carrier modulation method is selected due to its simplicity for implementation. It consists of a carrier wave which is basically a high frequency triangular waveform and a sinusoidal modulation signal, which amplitude varies depending on the speed command. These two signals are compared to generate a desired PWM output. The width of each PWM pulse is weighted by the amplitude of the sine wave at that instant. Therefore, the rms value of the voltage applied to the motor phase can be controlled by varying duty cycle of the PWM signal. A voltage of 5 V is selected to represent 1 pu value.

4.2 Soft-Start Circuit

The developed soft-start circuit consists of a difference amplifier (IC1:D) and an integrator (IC1:C). They are cascaded together to get a slow rising voltage ramp. Figure 2 shows the soft-start circuit and has a transfer function of

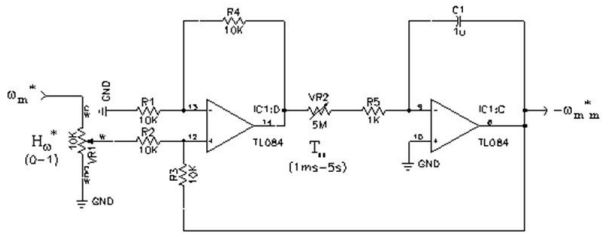


Figure 2. Soft-start circuit

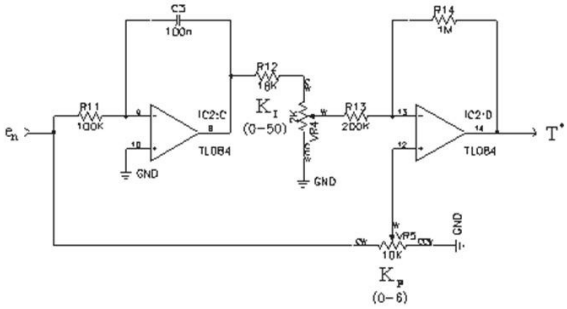


Figure 3. PI speed controller circuit

$$G_{ss}(s) = \frac{1}{1 + T_{ss} \cdot s} \tag{1}$$

where

$$T_{ss} = (VR2 + R5) \cdot C1 \tag{2}$$

is the soft-start time constant that can be varied with VR2 from 1 ms to 5 s. VR1 adjusts the commanded normalized speed input gain, H_ω^*. When VR1 is turned to its maximum position, the 5 V input commands the rated speed. In order to command the rated speed with a higher voltage, VR1 should be decreased accordingly.

4.3 PI Speed Controller

The PI speed controller shown in Figure 3 consists of IC2:C and IC2:D. Its transfer function is

$$G_c(s) = K_P + \frac{K_I}{s} \tag{3}$$

It produces the torque command, T^*. VR5 varies the proportional gain, K_P, from 0 to 6, and VR4 varies the integral gain, K_I, from 0 to 50. Since there is no simple way to determine these gains with the motor parameters, they should be adjusted empirically.

4.4 Torque Limiter

The torque limiter limits the torque, and consequently the motor current, to a safe level, and prevents the motor operation in the unstable region. The implemented torque limiter circuit is shown in Figure 4. It is formed around IC2:B and IC2:A. D1 does not allow the input

voltage to exceed the voltage at the wiper of VR6, and, therefore, VR6 adjusts the torque limit from 0 to about 2.4 p.u.. D2 does not allow negative input voltages, since this is a one quadrant drive and torque cannot be negative. The torque is proportional to the slip; the output of this circuit is the commanded slip speed in normalized unit, s^*.

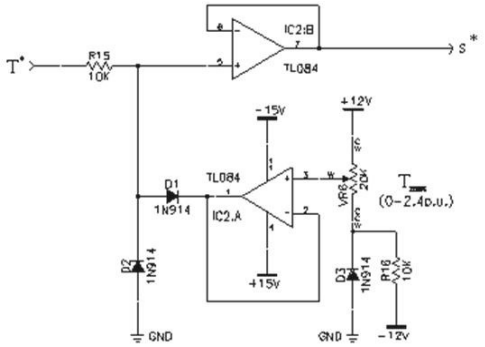


Figure 4. Torque limiting circuit

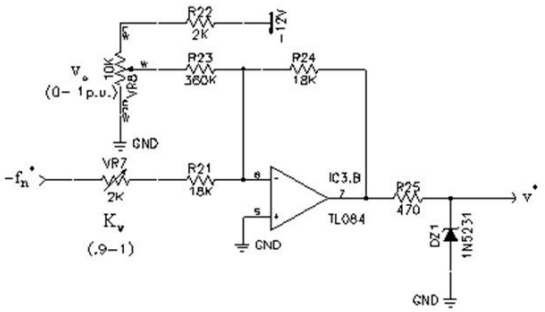


Figure 5. Voltage command schematic

4.5 Voltage Command Generation Circuit

The voltage command generation circuit is implemented with an inverting amplifier IC3:B and is shown in Figure 5. It produces the commanded normalized voltage from the commanded normalized synchronous frequency using the formula

$$v^* = v_o + K_v \cdot f_n^* \tag{4}$$

where v_o is the normalized offset voltage and K_V is the normalized frequency to normalized voltage constant. VR8 varies v_o from 0 to 0.1 p.u., and VR7 varies K_V from 0.9 to 1. At the output of this block, there is a 5.1 V zener diode which prevents commanded voltages higher than the rated level of 5 V. This causes the motor to operate in the flux weakening region for speeds higher than the rated one.

4.6 Voltage Controlled Oscillator

Figure 6 shows the voltage controlled oscillator (VCO) which is implemented with IC4 (XR 2207). The difference amplifier consists of IC3:C and IC3:D brings the input voltage to a value suitable for IC4. This block produces a TTL level square wave, v_{sqr}, with a frequency of f_a given by,

$$f_a = \frac{1}{R31 \cdot C6} \cdot \left[1 - \frac{(V_c - 6) \cdot R31}{6 \cdot R30} \right] \tag{5}$$

where V_c is the voltage at the output of IC3:C, and is given by

$$V_c = 2.4 \cdot V_{in} + 12 \cdot \frac{VR9_W}{VR9} \tag{6}$$

where $VR9_W$ is the resistance from the pot wiper to its end. VR9 adjusts the frequency to be 1024 times the commanded value.

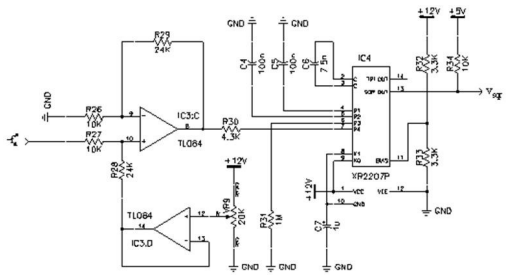


Figure 6. VCO schematic

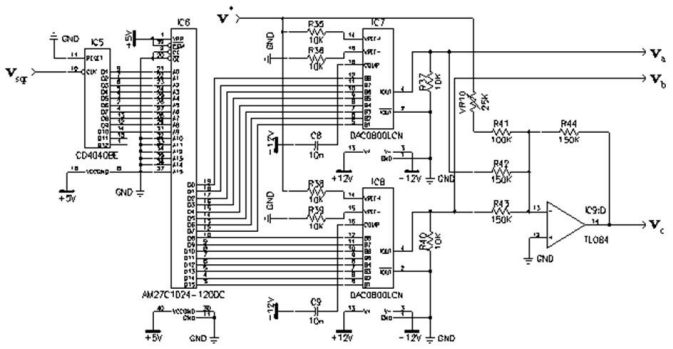


Figure 7. Sine wave generator circuit

4.7 Three-Phase Sine Wave Generation Circuit

The three-phase sine wave generation circuit produces three-phase sinusoidal waveforms according to the commanded normalized synchronous frequency and the commanded normalized voltage. Figure 7 shows the sine wave generator block. The signal from the VCO feeds a 12-stage ripple counter, IC5. The outputs of the counter's first ten stages, thus the $1024=2^{10}$, form a 10-bit address bus for a 16-bit output EPROM, IC6, where the sine waves for phases A and B are stored with 8-bit resolution for each phase. IC7 and IC8 are multiplying 8-bit DACs produce negative voltages down to -5 V. The amplitude and offset of the generated sine waves vary according to the commanded voltage signal, so that

$$v_a = -v^* \cdot \frac{1+\sin(2\pi \cdot f_s^* \cdot t)}{2} \tag{7}$$

$$v_b = -v^* \cdot \frac{1+\sin(2\pi \cdot f_s^* \cdot t - \frac{2\pi}{3})}{2} \tag{8}$$

where f_s^* is the commanded synchronous frequency. The voltage for the phase C is produced from the inverted summing amplifier circuit with IC9:D, as

$$v_c = -\tfrac{3}{2}v^* - (v_a + v_b) \tag{9}$$

VR10 balances the three-phase system eliminating any undesirable offset voltage from IC9:D.

4.8 Triangular Waveform Generation Circuit

The three-phase inverter is designed to operate at a switching frequency of f_S = 2.78 kHz. Therefore, the output of a carrier frequency generation circuit has the same frequency. Figure 8 shows the triangular carrier waveform generator circuit, which is formed around

IC11. This circuit produces a triangular waveform, v_{tri}, with a frequency of f_b which is given by,

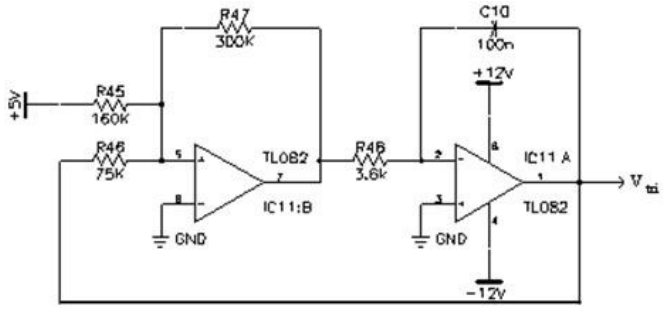


Figure 8. Triangular wave generator schematic

$$f_b = \frac{R47}{4 \cdot R46 \cdot R48 \cdot C10} \tag{10}$$

a peak-to-peak amplitude, V_m is given as

$$V_m = 2 \cdot V_{max} \cdot \frac{R46}{R47} \tag{11}$$

where V_{max} is the maximum output voltage of IC11 with 10 V, and an offset of V_{of},

$$V_{of} = 5 \cdot \frac{R46}{R45} \tag{12}$$

thus matching the output voltage range of the DAC0800.

4.9 Three-Phase PWM Generation Circuit

Figure 9 shows the three-phase PWM block comprising with IC10, IC9:B and IC9:C. Each of the three-phase sine waves is compared with the common triangular carrier waveform with two complementary comparators to produce the three-phase PWM signals: IC10:C and IC10:B for v_a, IC10:D and IC10:A for v_b, and IC9:C and IC9:B for v_c. The outputs of the comparators are v_{L1} - v_{L3} for the low-side and v_{H1} - v_{H3} for the high-side drive signals for the succeeding gate drive circuit.

The Multisim circuit diagram for the simulation of SPWM technique is shown in Figure 10. The schematic diagram shows the single phase only. The triangular carrier signal is common to all three-phase PWM generation circuitry. R1 and R2 are dummy loads to monitor resulting PWM signals. The simulation result which depicts the three-phase SPWM technique is shown in Figure 11(a) with the three-phase sine waves and triangular carrier waveform. The generated high-side PWM signal for the following gate drive IC, IR2130, is shown in Figure 11(b).

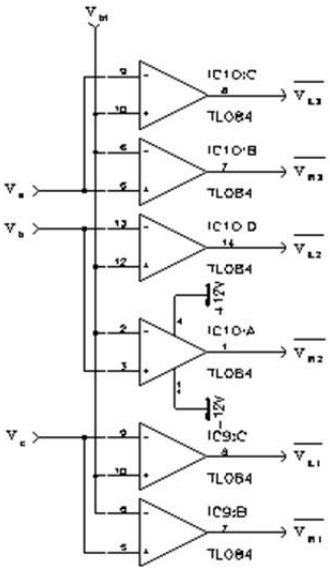


Figure 9. Three-phase PWM generation circuit

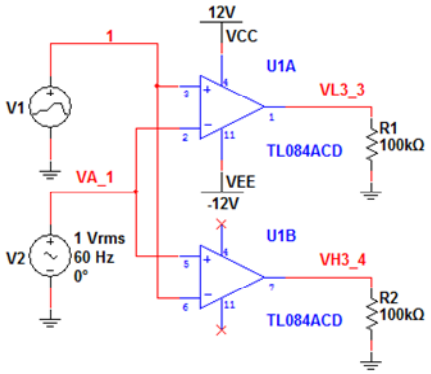
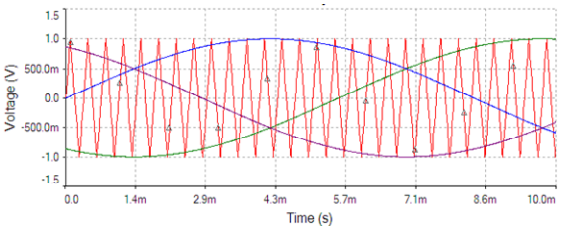
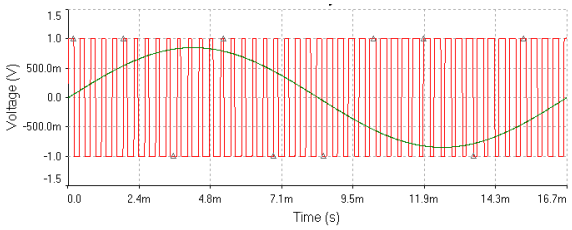


Figure 10 Multisim three-phase SPWM generation circuit (single phase only)



(a) Multisim simulation result with three-phase sine waves (60 Hz) and triangular carrier waveform (2.78 kHz)



(b) Three-phase SPWM signal for the phase A

Figure 11. Multisim simulation result of the normalized three-phase PWM signals with SPWM technique

4.10 Gate Drive Circuit

A high voltage three-phase gate driver IC, IR2130 from International Rectifier is used for interfacing gate drive signals with MOSFET power switches. Figure 12 shows the gate drive circuit which is implemented with IC12 (IR 2130). The PWM signals are limited to a 0 to 5 V range, and fed to the gate driver circuit, IC12, which interfaces them to the power switching devices. IC12 contains three floating and three ground-referenced drivers, and provides deadtime between the high- and the low-sides, and current limiting. VR11 adjusts the dc bus current limit value from 2 A. It should be adjusted so that the instantaneous bus current does not exceed the rated instantaneous switching power device current. v_{G1} - v_{G6} are

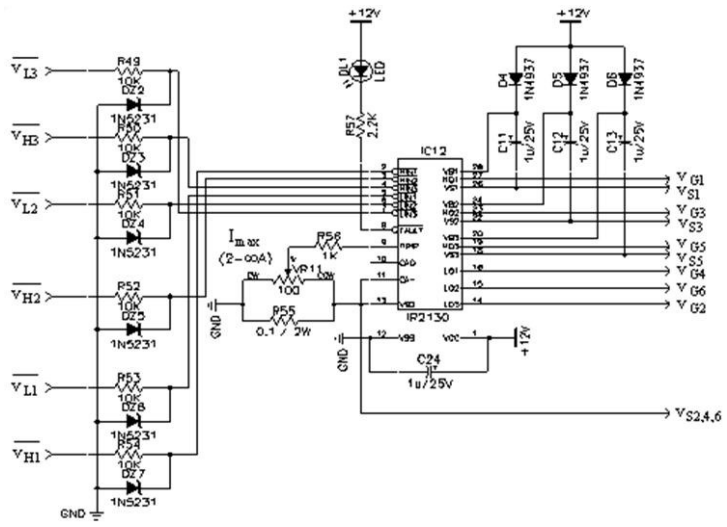


Figure 12. Gate drive circuit

connected to the gate terminals of power switching devices, and v_{S1} - v_{S6} to the power devices' source terminals. The three-phase inverter circuit consists of six IRF840 Power MOSFET devices in this study. But integration of those power devices by replacing with an intelligent power module which encase the dedicated gate drive circuit and protection circuit may provide better thermal management, smaller footprint, and less electromagnetic interference (EMI) noise emission.

5. Loss Evaluations and Cooling Design

5.1 Losses in the Converters

The inverter operates at a switching frequency f_S = 2.78 kHz. The resistors that are in series with the devices' gates set the switching time to about 0.5 μs. Assuming the dc bus voltage is constant at

$$V_{BUS} = 230 \cdot \sqrt{2} \ V \tag{13}$$

the three-phase inverter losses are modeled as:

$$\begin{aligned} P_{INV} &= 3 \cdot \left(\tfrac{1}{2} \cdot V_{BUS} \cdot I_M \cdot f_S \cdot \left(t_r + t_f \right) + \tfrac{1}{2} \cdot V_{BUS} \cdot I_M \cdot f_S \cdot t_{rr} + {I_M}^2 \cdot R_{DS} \right) \\ &= 1.98 \cdot I_M + 3.57 \cdot {I_M}^2 \end{aligned} \tag{14}$$

where I_M is the motor current, t_{rr} the reverse recovery time of the antiparallel diodes of the power MOSFET switching device, and R_{DS} is the ON resistance of the power devices.

The loss model of the front-end full-wave bridge rectifier circuit is:

$$P_{BR} = 2 \cdot V_D \cdot I_{IN} = 2 \cdot V_D \cdot \frac{P_{IN}}{V_{IN}} = 2 \cdot 0.7 \cdot \frac{P_{IN}}{230} = 0.0061 \cdot P_{IN} \quad (15)$$

where V_D is the voltage drop across one of four bridge rectifier diodes, I_{IN} is the input current, and P_{IN} is the input power. The drive efficiency is derived from the inverter losses and the bridge rectifier losses. Based on these, the maximum inverter and bridge rectifier losses are estimated to be 40.8 and 6.21W, respectively, giving total losses of 47W.

5.2 Cooling Design

Based on the estimation of 47W losses, the compactness requirement in the drive packaging requires the smallest heatsink with forced air cooling. A compact heatsink which could satisfy all the requirements including the most crucial one of low-cost until a heatsink with dense small thin fins and allowing a turbulent air flow is utilized in this design and layout to meet the compactness requirements.

6. PCB Layout Design and Final Assembly

Based on the heatsink dimension of 2.4 inches square and the final package volume requirement of 100 cubic inches, it became necessary to develop the layout of the power, controller, dc link filter, power supplies, fuses and connector around these specifications. The controller boards were split into two boards with dimensions of 2.45" × 5.1" and the power board connections were arranged in a printed circuit board (PCB) of 2.87" square. The drive circuit is divided into three double-sided PCBs, namely control board, driver board, and power board, as shown in Figure 13. The control board and driver board are implemented on the 5.0"× 2.4" PCBs. They contain the housekeeping power supply and the PI controller and the sine wave generator, and the PWM circuit and the gate drive IC, respectively. The power board (2.8"× 2.8") contains the bridge rectifier, the power devices, and the rest of the power circuit. The bridge rectifier and the power devices are mounted on the 2.4"× 2.4"× 0.5" heatsink, which also has a small fan attached to it. The three PCBs are assembled to form a 'Π' with the control board and the driver board at the sides, and the power board at the top, so as to enclose the dc bus electrolytic capacitors. A 6.0"× 4.3"× 2.9" enclosure was designed for the drive as follows: The top two pieces are folded to form two 'L's along the dotted line. When put together, they form a box whose front and back are the other two pieces. There is a hole in the middle of the front piece for mounting a potentiometer, if one is used to give the speed command.

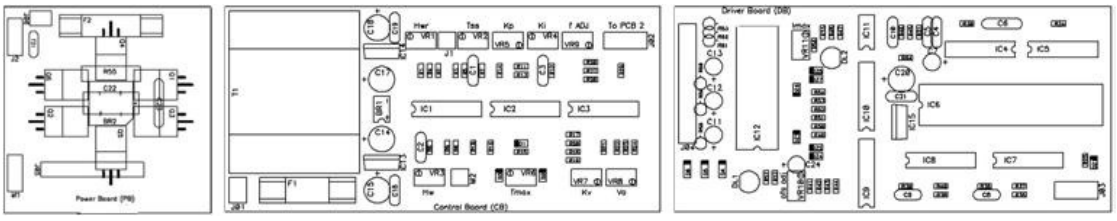


Figure 13 Proposed three PCBs to enclose all electronic circuitry
(from left: power, control, and driver boards)

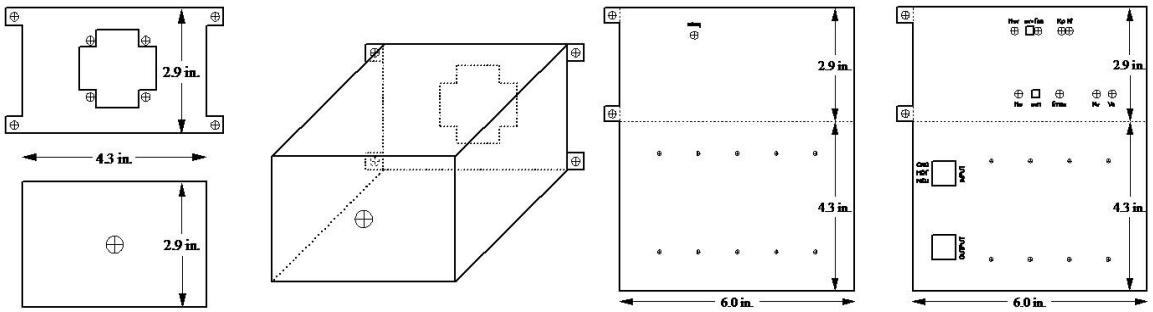


Figure 14. Proposed enclosure design

Figure 15. Comparison of the developed inverter (left) with a commercial one

The four holes at the edges of the rear piece are used for the mounting of the drive. The final enclosure assembly had the dimensions of 4.3"x 2.9"x 7" including heatsink and fan with an overall packaging volume of 87 cubic inches thus satisfying the packaging specification of less than 100 cubic inches. The proposed enclosure design is shown in Figure 14 and the prototype VSD is compared with Toshiba's VF-SX inverter in Figure 15. The size of the Toshiba's inverter is 4.1"x 5.9"x 4.7" (approximately 114 cubic inches) with one hp output rating and contains many extra functions which are not necessary for the low-cost fan/pump applications. The designed inverter is comparable to a commercial one in enclosure size.

7. Experimental Results

Experimental results on a one hp induction motor using the prototype VSD are presented in this section. The measured motor current waveform and its fast Fourier transform (FFT) result are shown in Figure 16. The FFT shows a strong fundamental frequency, 60 Hz, component with negligible harmonics. The current ripple in the motor current waveform can be reduced by increasing the frequency of the PWM. The overall efficiency of the motor drive is both calculated using procedures outlined in [11] and measured as shown in Figure 17 for a fan load. The efficiency of both methods shows a close match over the entire speed range. Figure 17(b) shows the predicted and measured induction motor and drive efficiencies that contributed to the system efficiency curves shown in Figure 17(a).

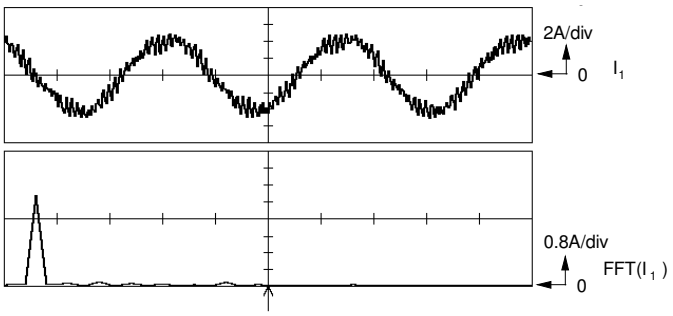
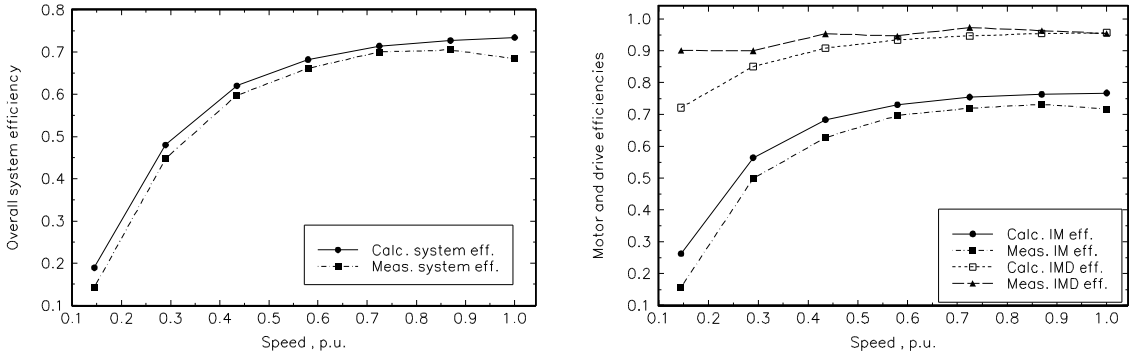


Figure 16 Motor current (Horizontal: 5 ms/div) and FFT (Horizontal: 100 Hz/div)



(a) Overall system (b) Motor and inverter

Figure 17. Predicted and measured efficiencies

8. Topics for Electric Motor Drives Course

With the prototype IMD, the following topics are valuable for the electric motor drives course: principles and operations of the three-phase rectifier, SPWM, three-phase inverter, V/Hz control technique, three-phase sine wave generation, PI controller, gate drive circuit, soft start circuit, torque limiting circuit, VCO, and triangular waveform generation circuit. The layout design of the developed circuitry on PCB to optimize the power dissipation and EMI emission is very useful for the development of a VSD in the real world. Tuning and adjustment of the VSD provides plenty of hands-on experience to the students.

9. Conclusion

A high density package of less than 100 cubic inches, one hp IMD with discrete analog, and digital components have been designed, implemented and tested for emerging high volume VSD applications. The design details and considerations of the controller, converters, their layouts and packaging, thermal design and overall packaging were systematically developed to assist in the development of other drives of various sizes. The overall VSD system efficiency and induction motor efficiency are obtained analytically and empirically. Both results were well matched with each other over the entire motor speed range. In a conclusion, various teaching components are identified for the electric motor drives course.

References

[1] R. Krishnan, "Electric Motor Drives: Modeling, Analysis and Control," Prentice Hall, 2001

[2] Padmaraja Yedamale, "Speed Control of 3-Phase Induction Motor Using PIC18 Microcontrollers," AN 843, Microchip Technology, 2002.

[3] Dave Wilson and Bill Lucas, "Ready-to Use AC Induction Motor Controller IC for Low-Cost Variable Speed Applications," Freescale Semiconductor White Paper, MC3PHACWP Rev. 0, October 2005.

[4] Ali Keyhani, Mohammad Marwali, Lauis Higuera, Geeta Athalye, and Gerald Baumgartner, "An Integrated Virtual Learning system for the Development of Motor Drive systems," IEEE Transactions on Power Systems, vol. 17, no. 1, pp. 1-6, February 2002.

[5] Carlo Cecati, Antonio Dell'Aquila, and Marco Liserre, "A Novel Three-Phase Single-Stage Distributed Power Inverter," IEEE Transactions on Power Electronics, vol. 19, no. 5, pp. 126-1233, September 2004.

[6] Jacinto Jiménez-Martinez, Fulgencio Soto, Esther de Jódar, Jose Villarejo, and Joaquin Roca-Dorda, "A New Approach for Teaching Power Electronics Converter Experiments," IEEE Transactions on Education, vol. 48, no. 3, pp. 513-519, August 2005.

[7] Robert Balog, Zakdy Sorchini, Jonathan Kimball, Patrick Chapman, and Philip Krein, "Modern Laboratory-Based Education for Power Electronics and electric Machines," IEEE Transactions on Power Systems, vol. 20, no. 2, pp.538-547, May 2005.

[8] S. Shirsavar, Benjamin Potter, and Isabel Ridge, "Three-Phase Machines and Drives – Equipment for a Laboratory-Based Course," IEEE Transactions on Education, vol.49, no. 3, pp.383-388, August 2006.

[9] Erkan Mese, "Project-Oriented Adjustable Speed Motor Drive Course for Undergraduate Curricula," IEEE Transactions on Education, vol.49, no. 2, pp. 236-246, May 2006.

[10] Anibal Almeida, Fernando Ferreira, and Dick Both, "Technical and Economical Considerations in the Application of Variable-Speed Drives with Electric Motor Systems," IEEE Transactions on Industry Applications, vol.41, no. 1, pp. 188-199, January/February 2005.

[11] R. Krishnan, D. Diamantidis and S. Lee, "Impact of Power Factor Correction on Low Power Inverter-Fed Induction Motor Drive System," IEEE Power Electronics Specialists Conference, pp. 593-598, 1995.

[12] J. Zhao and J. Liu, "Modeling, Simulation and Hardware Implementation of an Effective Induction Motor Controller," International Conference on Computer Modeling and Simulation (ICCMS 2009), pp. 136-140, February 20-22, 2009.

[13] L. Xue and J. Liu, "Simulation and Experiment of Induction Motor Controller," IEEE International Conference on Computer and Automation Engineering (ICCAE 2009), pp. 54-58, March 8-10, 2009.

[14] C. Kamble, J. Chaudhari, and M. Aware, "Digital Signal Processor Based V/f Controlled Induction Motor Drive," IEEE Third International Conference on Emerging Trends in Engineering and Technology, pp. 345-349, November 19-21, 2010.

[15] M. Arrofiq, N. Saad and M. Karsiti, "Performance of a PLC-based Hybrid Fuzzy Controller for PWM-driven Variable Speed Drive with Constant V/Hz Ratio," IEEE International Conference on Intelligent and Advanced Systems (ICIAS 2010), pp. 1-6, June 15-17, 2010.

Biography

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