CLDT: A Combinational Logic Design Interactive Web-based Tool

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ABSTRACT

A lack of resources exists outside of the classroom to aid electrical and computer engineering students in the understanding of the basic fundamentals of digital design topics. The Combinational Logic Design Tool (CLDT) provides students with the ability to gauge their own progress in their classes while allowing them to be self as well as lifelong learners. CLDT is designed to work with the students' base knowledge and through practice improve this knowledge and expand it. It is also designed to help students develop their self-monitoring skills. No purely assessment tools exist in the area of digital logic design and hence CLDT is expected to fill a large void in terms of online assessment/practice tools. This paper describes research that produces a complete interactive online assessment tool to assess students' knowledge of the process of designing and implementing a combinational logic circuit.

INTRODUCTION

Although different forms of technology based education exist, there exists no application that is considered to be an online *practice tool* for students in Electrical and Computer Engineering. A need exists for a tool that would be perceived and used by students as a tool that helps them *"practice"* what they have learned in the classroom. The Combinational Logic Design Tool (CLDT) implements a novel approach to online learning. This approach is the development of *web-based online practice tools*. The idea behind these tools is to provide a venue for students to practice what they have learned in the classroom. This is achieved through randomly generating problem statements (not randomly choosing from a list) and allowing students to solve these problems through a step-by-step process. The tool performs a *Just-In-Time (JIT) assessment* of the student's response and the student is informed at the end of each step whether their response is correct or incorrect, however, a solution is *not* provided to them. In order to ensure a student completely understands a concept, the solution cannot simply be provided and the problem needs to be solved in a step-by-step fashion. The tool does not provide solutions in order to guarantee that students use this tool as a form of practice tool not a tool to aid

them in solving their homework assignments. The design of the tool provides endless problems for students to *practice* combinational logic design.

This paper discusses the CLDT tool and its' functionality. The paper presents the tool including the three sub-tools which mimic the three stages required for the design of a combinational logic circuit, namely: truth tables, Karnaugh Map minimization, and circuit design. Digital Logic Design was chosen as the subject matter for implementation of this novel tool design due to the fact that it is a core subject in Electrical, Electronics, Computer Engineering and Technology as well as Computer Science degrees nation and world wide. It is a core required course in both 4 year and 2 year colleges and universities. Digital Logic Design is also a pre-requisite to subjects like Microprocessors, Computer Architecture, Microcontrollers and Digital Integrated Circuits.

BACKGROUND

The main objective of the Accreditation Board for Engineering and Technology (ABET) [1] is to improve the overall quality of engineering education. This can be done through improving communication skills, encouraging team work, and providing an environment that allows students to acquire the knowledge they need through technology as well as traditional methods of learning. The use of computer technology in engineering education has been a topic of ongoing interest for the last few decades. Computers have become an integral component of our lives and it only seems natural to make the most of them in the educational process of engineers. Computers have become an essential computation tool for students and computer based learning has proven to be an accepted learning practice that can improve the educational process for students.

Teaching methods in an engineering classroom vary from the traditional black/white board style to the completely online style of teaching. Use of electronic media in classroom lectures (e.g. using Power Point presentations in class as well as posting them on a web-site), are received well by students [2], even though they may be time consuming in their preparation. Research [3] has indicated that students' grades improved with the introduction of non-traditional forms of teaching. This conclusion was reached by conducting a survey on the use of four different forms of instruction, namely: Traditional, Interactive Video, Web-assisted, and Streaming media. However, students showed a preference for the Web-assisted format over the other technologies. Ongoing research [2-5], suggests that web-based lecturing formats are highly effective and interesting to students.

The Commission on Behavioral and Social Sciences and Education (CBASSE) stated in their publication "How People Learn: Brain, Mind, Experience, and School: Expanded Edition (2000)" that since interactive environments are common nowadays, "it is now easier to create environments in which students can learn by doing, receive feedback, and continually refine their understanding and build new knowledge" [5]. These new technologies help in visualization as well as provide access to a wealth of knowledge through digital libraries.

"The interactivity of these technology environments is a very important feature for learning. Interactivity makes it easy for students to revisit specific parts of the environments to explore them more fully, to test ideas, and to receive feedback. Non-interactive environments, like linear videotapes, are much less effective for creating contexts that students can explore and reexamine, both individually and collaboratively." [5]

Within the electrical and computer engineering curriculum, fundamental theories and concepts are taught that provide tools to be used by students in their upcoming careers. These topics are traditionally taught in a classroom by professors engaging in discussion with the student. However, a lack of resources exists outside of the classroom to aid the student in the understanding of these topics. Software packages [6-8] that allow for the simulation of logic circuits exist and are excellent for analysis and simulation; a great aid to the experienced engineer but provides little help in the education process of the student. Other systems [9-13] provide questions for students to solve and submit answers to. These systems are little more than computerized homework helpers/solvers that do not allow the student to solve the problem themselves and see whether they have applied their newly acquired knowledge correctly [14].

It becomes apparent that other tools are necessary to help in the education of students outside of the classroom. A form of e-learning is needed where the student is allowed to interact with a web-based tool as he or she would interact with a professor in a classroom. In a regular classroom setting, when a student starts working on a problem, he/she does so by going through a specific sequence of steps at the end of which would be the final solution or design. If the student faces a problem along the way, the professor is approached to let the student know if he/she is on the right track.

The Interactive Karnaugh Map Evaluator Tool [15] was originally developed by the author (Morsi) to serve as a web-based interactive application that allows students to practice the knowledge they acquired in the classroom as they would in the presence of their professor. The Interactive Karnaugh Map Evaluator is a tool to allow students to practice the minimization process of expressions in digital logic (a core lower division course for Electrical, Electronics, Computer Engineering/Technology and Computer Science).

CLDT

CLDT's [19] main objective is to provide JIT web based assessment. It is composed of three main components (sub-tools) shown in Figure 1. CLDT includes a Truth-Table evaluator sub-tool which is the default module, a Karnaugh Map (KMap) sub-tool, which is an upgrade to the preexisting tool (the Interactive Karnaugh Map evaluator tool [14]), and the Circuit Design sub-tool. These three sub-tools form a complete "just-in-time" assessment tool for students to practice procedures they have learned in the classroom. Each sub-tool can operate as a stand alone tool, capable of randomly generating its own appropriate problem statements. The KMap and circuit design sub-tools also have the capability of retrieving the results achieved in the preceding sub-tool. This allows the

user to transition within CLDT for a complete design experience. The random problem generation process makes it highly unlikely that a student will get the exact question they might have had for a homework assignment. However, it will produce a problem statement that may closely resemble a homework assignment statement. This would encourage the student to practice and understand it rather than memorize a solution for short term use. CLDT also has the advantage of linking the three sub-tools in sequence which allows the students to start from the one sub-tool and continue that question straight to the next.
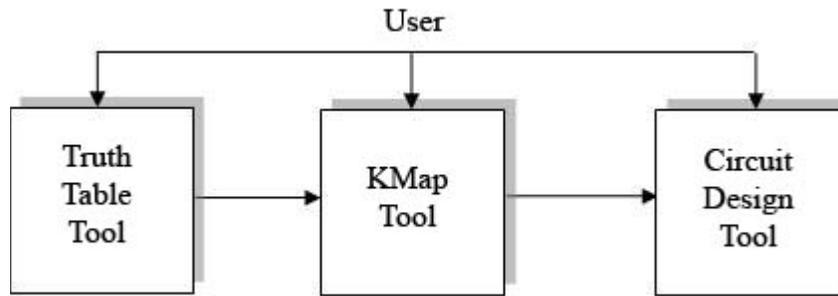
Figure 1: CLDT User tool option.

1. The Truth Table sub-tool

The truth table sub-tool's Graphical User Interface (GUI) allows the user to:

    a. Select the KMap size (2,3,4, and 5 variables)
    b. Select 'Don't Care' conditions (0, 10, 20, and 33%)
    c. Create the Truth table

Once the table is generated, the user is allowed to practice the transfer of truth tables into KMaps. The user is required initially to determine the number of cells needed to generate a KMap for the given truth table. If the answer is incorrect, the user is prompted for another answer. Once the user provides a correct response, the map is generated and the user is now able to populate the map. The tool allows for both novice and expert users. For the novice user, the tool will allow the user to highlight the output that will be used to populate the map. The user is then supposed to fill in the appropriate cell in the map. As soon as the answer is input, the tool will detect it and respond with a 'correct' or 'incorrect' prompt. The reason this methodology is used is to allow for the novice user to know step by step how they are doing in their design process. In the expert mode (as shown in Figure 2), the user is allowed to completely populate the KMap and then submit the answer for assessment.
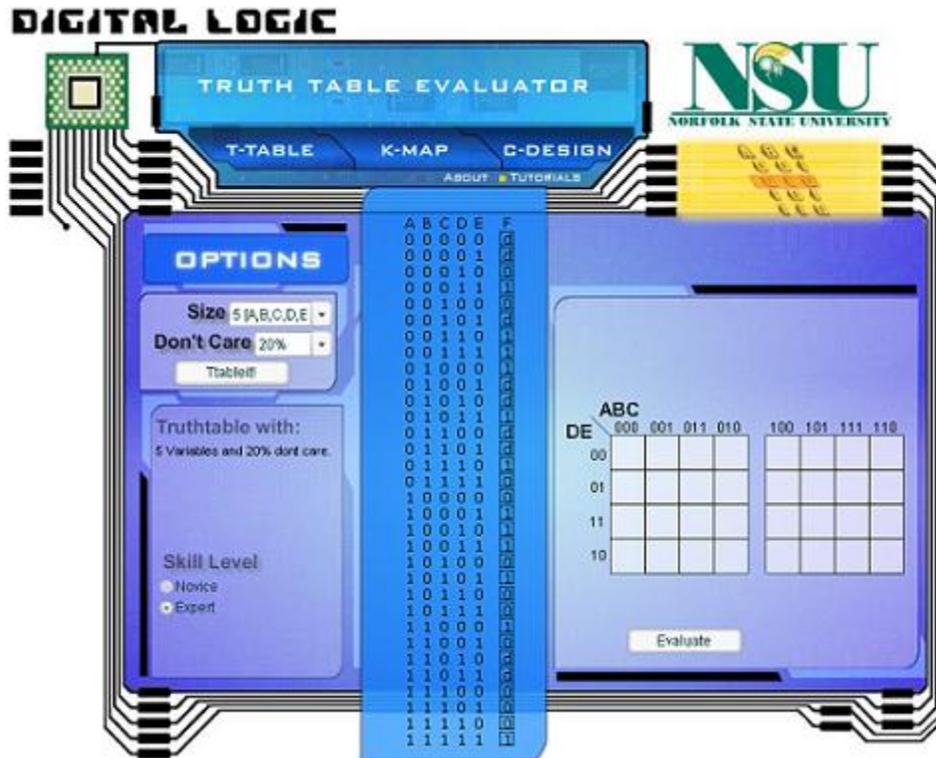
Figure 2: A 5 variable truth-table with 20% 'don't care'
conditions converted to a KMap cell map

2. *The KMap sub-tool*

The Karnaugh Map Evaluator sub-tool's primary function is the simplification of functions using Kmaps. The tool has been modified and re-implemented using Macromedia Flash Action Script in order to place it as a component of CLDT. The user is presented with randomly generated Karnaugh maps and is required to create minimized expressions. Figure 3 shows the GUI design for the KMap sub-tool. The user starts by choosing the number of inputs and percentage of 'don't care' conditions for the KMap (as was the case with the truth table sub-tool).

The tool allows for both Product of Sums (POS) and Sum of Products (SOP) expressions which would be selected before the user selects the 'KMap it' function. After the user selects the required options, an interactive session is displayed (Figure 4).
In this session the user is expected to minimize the KMap by selecting appropriate cells and generating the product/sum terms (depending on if the session is in the SOP/POS mode). The product/sum terms are placed in the "Term Equation" section. The user then selects the "Add to Final Equation" function for the tool to start the assessment process on this term. The user is then prompted of the outcome. If the term is correct it is placed in the Final Equation text box, the highlighted cells change color to indicate their grouping, and the user is then allowed to select a new group of cells. This process is repeated until all pertinent cells are selected. Once this is done, the user selects

"Evaluate" to determine if the final expression generated is in fact minimal. This minimality check feature is non-existent in available online tools [9-13].
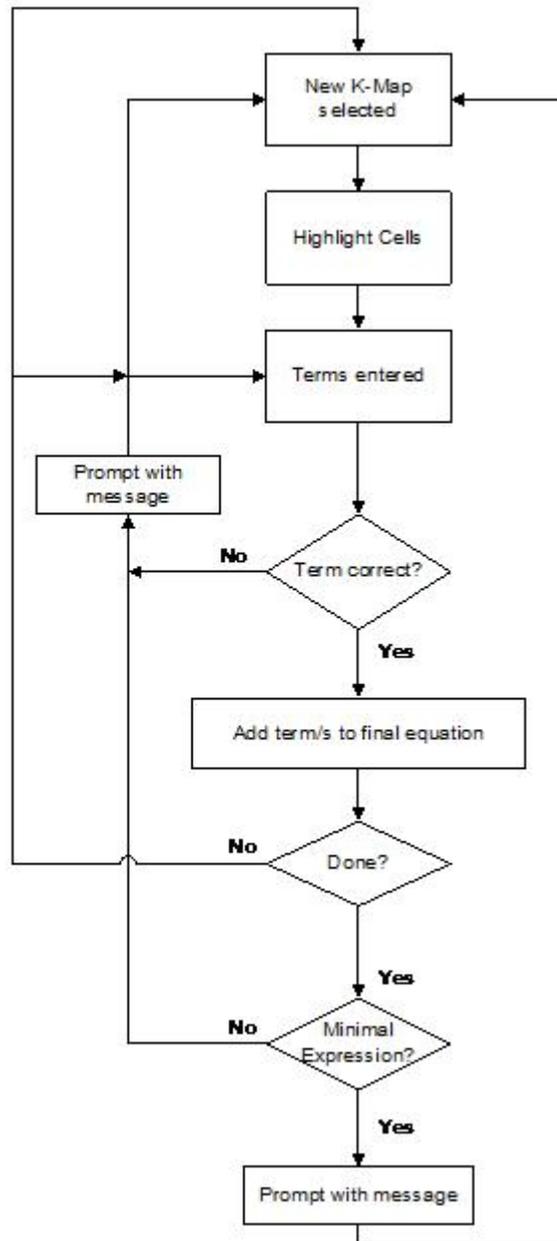

Figure 3: GUI Flowchart [14]

The KMap sub-tool also allows for the experienced user to directly insert the minimized expression in the "Final Expression" text box.
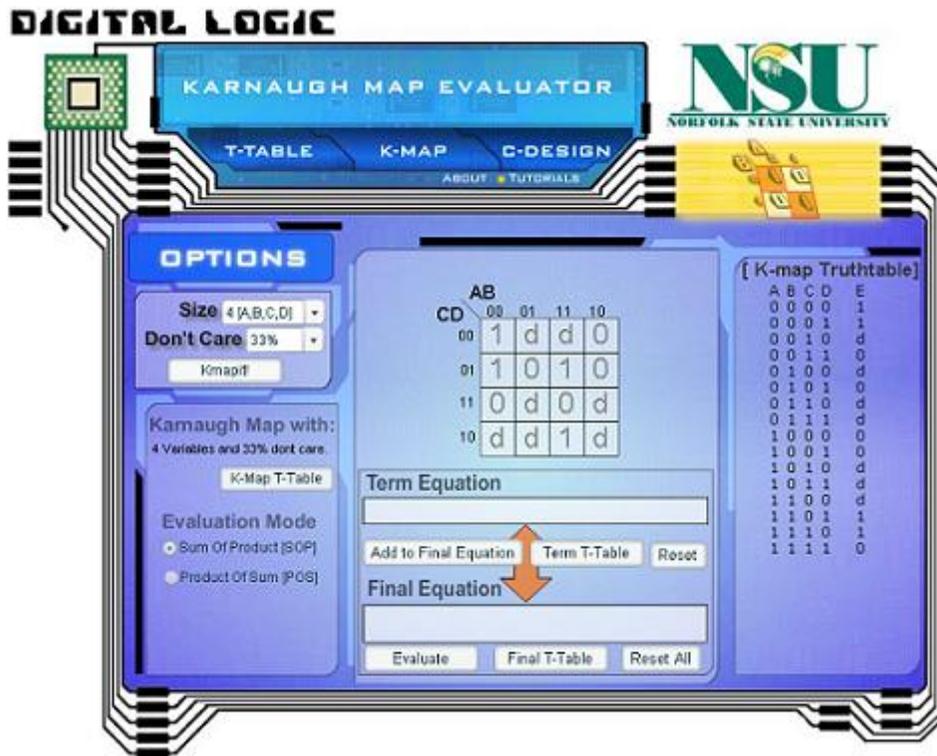
Figure 4: Interactive session in the KMap sub-tool showing a 4 variable map with 33% 'don't care' conditions

3. *The Circuit Design sub-tool:*

This is the third sub-tool in CLDT. Again, this sub-tool operates in two ways, retrieve answers from the previous stage or randomly generate problem statements in the current stage. In the former, the tool will accept the answer provided by the user from the KMap phase and allow the user to design the circuit using AND, OR, and NOT gates. In both cases, the user will have the option of choosing the number of inputs to use on each gate. After the user has implemented the circuit, the tool will assess the answer and prompt the user with a 'correct' or 'incorrect' response. Figure 5 shows a correctly implemented minimized expression. A special feature of this sub-tool is that it will provide the user with information on each gate being inserted in the circuit design showing what type of gate it is and the output this gate would have with its current connections. This feature is presented to aid the novice user as he or she is designing their circuit and again provide a step by step check status of their design. The sub-tool also checks for minimal number of gates being used in the design. If a design is correct but used more gates than necessary, the tool will prompt the user with this conclusion. It allows for both SOP and POS implementations and expressions. A 'line' connect option is available to help designs that would involve a single variable and also to help in design clarification when the design involves a large number of gates. Appendix A shows a completed example of the design process using CLDT.
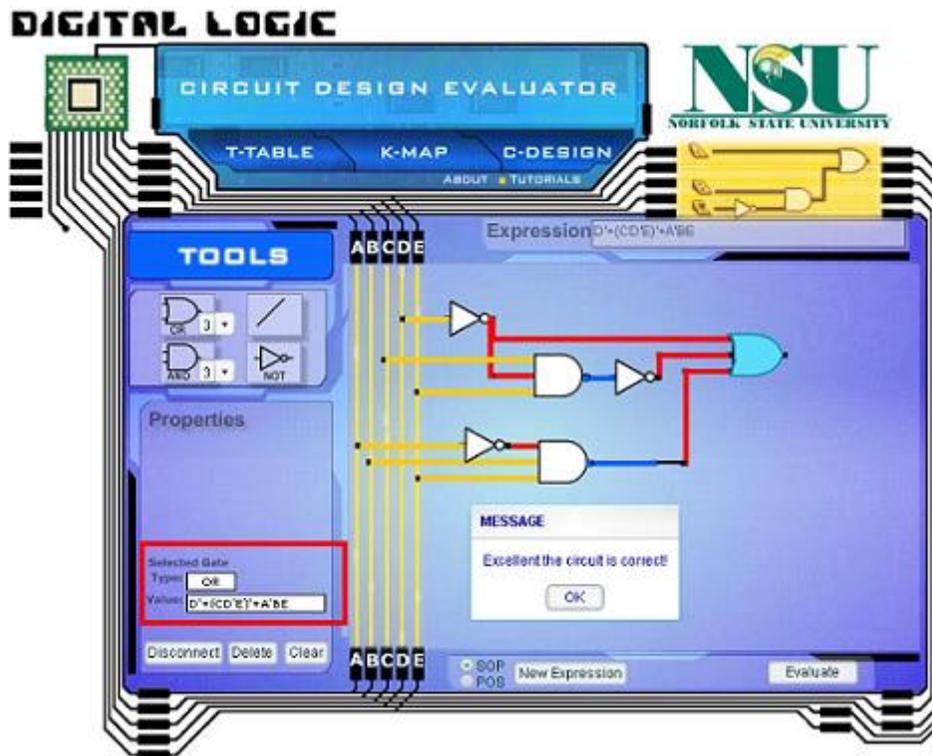
Figure 5: Example of a correct circuit for a minimized expression.

IMPACT ON STUDENT LEARNING

Use of CLDT by students outside of the classroom will have significant impact on their retention of the knowledge gained in the classroom. The Interactive Karnaugh Map Evaluator tool [15] was introduced to students at Norfolk State University (NSU) in the Fall semester of 2004 and an initial survey of 13 students showed that 93% of the students agreed that the tool re-affirmed the knowledge they gained in the classroom, 77% liked the fact that the tool was online and available to them whenever they needed it, and 85 % stated that they would like to see similar tools to aid them in their learning process for their other classes. Some comments from this survey had noted the need for a tool to help students practice other aspects of combinational design as well as sequential design. A detailed assessment of CLDT will be performed over the Spring 2008 semester across two campuses in order to determine the full impact of the tool on knowledge retention.

FUTURE DIRECTIONS

A future direction for this work is to develop the Sequential Logic Design Tool (SLDT). Once completed, Digital Logic Design Tool (DLDT) will be a tool that houses both combinational and sequential design practice tools. SLDT is a tool that will aid undergraduate students in Electrical, Electronics, and Computer Engineering and Technology as well as Computer Science majors in the development and enhancement of

their skills in Sequential Logic Design. Figure 6 shows the general SLDT sub-tool structure. It mimics the current CLDT structure by having three independent yet sequential sub-tools: State Diagram Generator Tool, State Table Tool, Circuit Design Tool (to feature the design using both combinational and sequential elements, namely D flip flops).
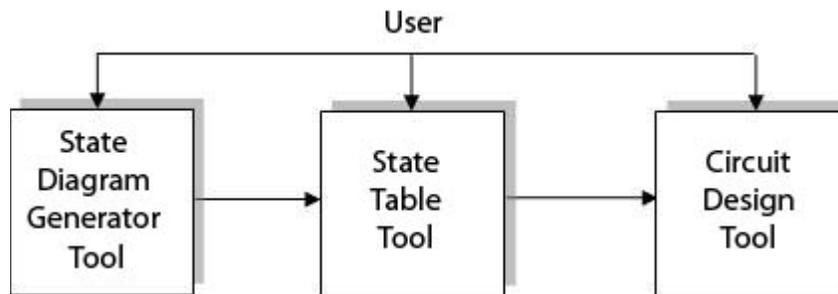

Figure 6: SLDT User tool option.

CONCLUSIONS

The Combinational Logic Design tool has been developed and has been shown to possess the ability to fill a void that currently exists in the online "practice" tool category. CLDT is a "Just in Time" assessment and practice tool that allows students to practice the digital logic design concepts they have learned in the classroom. This is done through a step by step process to allow the students to gauge their progress as well as allow them to become self monitoring. The tool is currently available online (www.cldt.ece-edu.com) in order to allow any student the ability to access and successfully make use of this tool. The tool should be of significant value to both novice and experienced students. Future work by the authors will address the assessment aspects of this tool.

ACKNOWLEDGEMENTS

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BIOGRAPHIES

Dr. RASHA MORSI is an Assistant Professor in the Department of Engineering and Director of the Center for Gaming and Simulation (CGS) at Norfolk State University. Dr. Morsi received her B.Eng degree from King's College, University of London, in 1991. She received an ME in Computer Engineering and a Ph.D. in Electrical and Computer Engineering from Old Dominion University, in 1996 and 2002 respectively. Her recent funding and research activities include port simulations, e-learning, educational gaming, and wireless communication networks and protocols.

LINTON RUSSELL received his Bachelor and Master of Science degrees in Computer Science from Norfolk State University in 2004 and 2006 respectively. Mr. Russell is currently a Software Developer with America Online (AOL).

APPENDIX A

EXAMPLE OF CLDT FUNCTIONALITY

Truth Table sub-tool

The default module is the Truth table sub-tool. The user selects the options and then selects "TTable it!" and the truth table interactive session starts as shown in Figure 7.
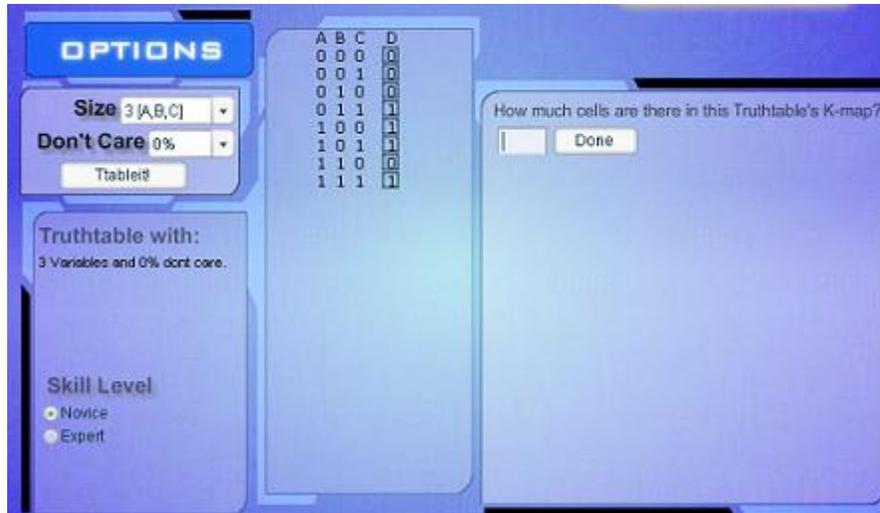
Figure 7: Truth Table module of CLDT

The user then enters the number of cells required for the corresponding KMap. Figure 8 shows the resulting empty KMap.
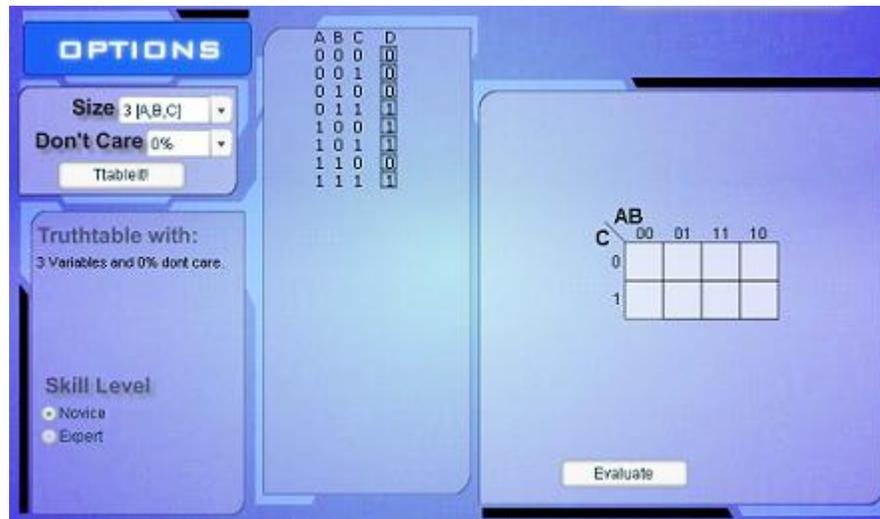

Figure 8: 3 variable, 0% don't care KMap generated

The tool is now set at the 'novice' level, so the user needs to select an input/output combination on the truth table and enter the corresponding output into the appropriate cell on the KMap (Figure 9(a)). An example of the response the user will receive in case of an incorrect cell selection is shown in Figure 9 (b).
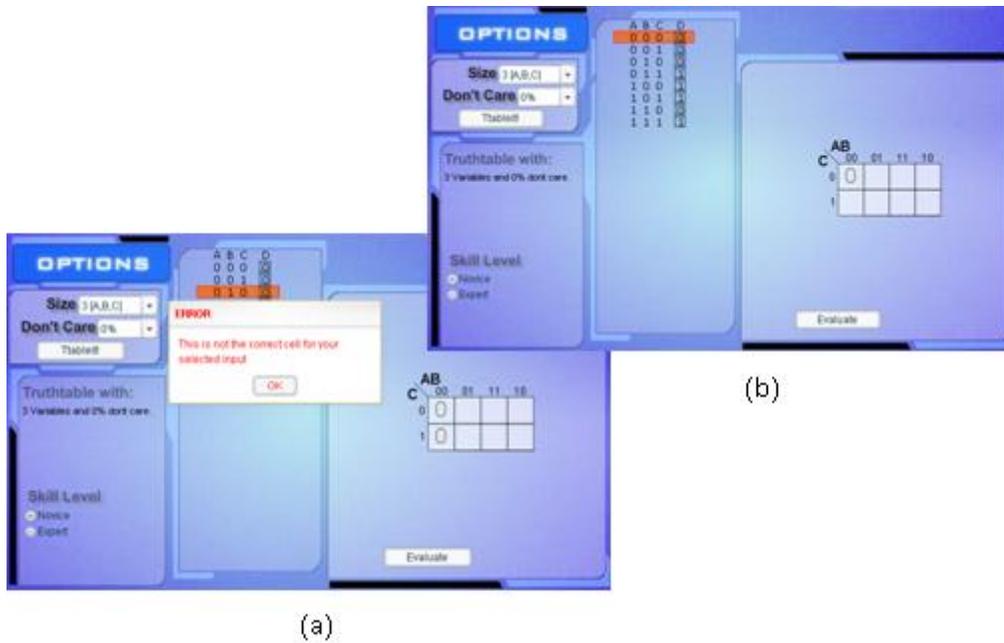
Figure 9: Truth table entry into the KMap

Once the KMap cell entry process is completed, the user evaluates the Map as shown in Figure 10 (a). The "Minimize" button then appears which is then selected and takes the user to the KMap sub-tool (Figure 10(b)).
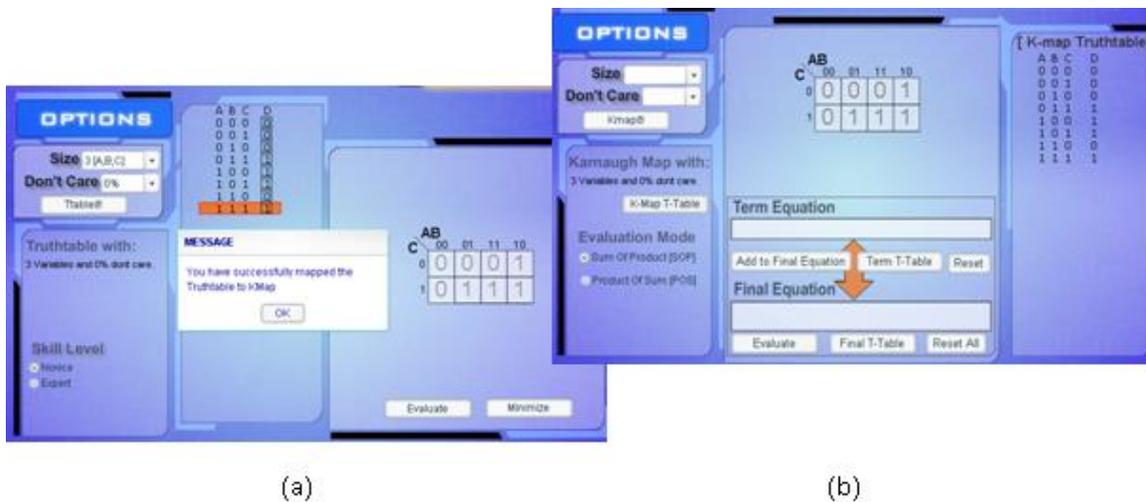
Figure 10: Successful truth table to KMap cell entry

KMap sub-tool

The user here is required to select the appropriate cells (groups) and generate the corresponding product term for evaluation. Figure 11(a) shows a group being selected and the corresponding product term (BC) entered in the "Term Equation" text box. The

user then selects "Add to final expression" and if the term is correct, it is added to the "Final Expression" text box (Figure 11(b)).
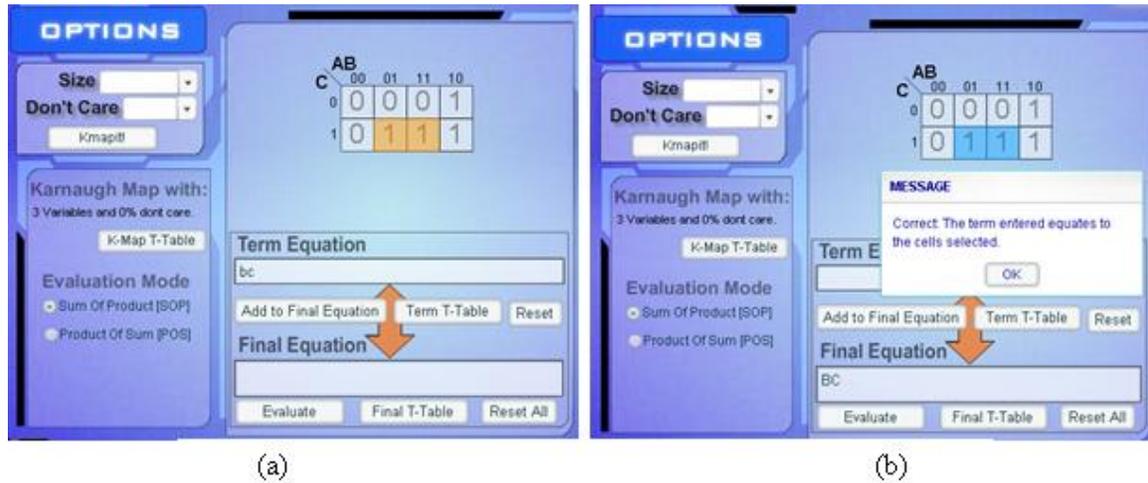

Figure 11: Cell grouping and term generation

Once the whole map is grouped successfully, the user selects the "Evaluate" button to check for minimality and the response is provided as shown in Figure 12. The 'Draw Circuit' button appears which allows the user to now implement the minimized expression using the C-design tool.
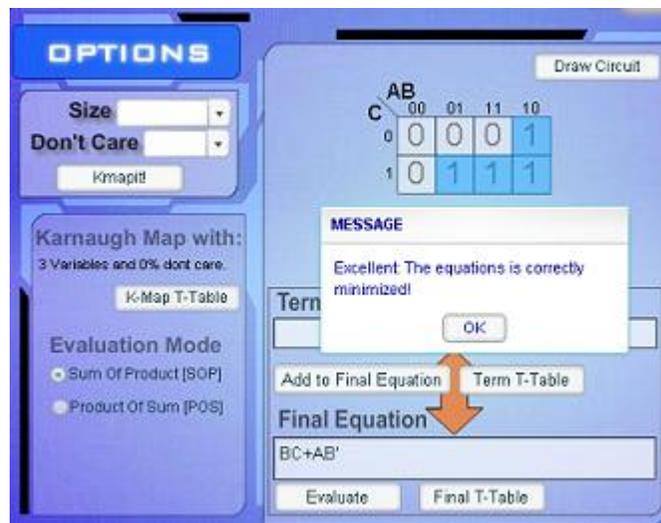

Figure 12: Minimized KMap

Circuit Design sub-tool

The user is now allowed to implement the expression using AND, OR, and NOT gates only. The minimized expression from the KMap stage is viewed in the 'Expression' textbox as shown in Figure 13. Once the implementation is complete, the user selects

'Evaluate', and the tool provides the result of the circuit assessment. The final evaluated design is also shown.
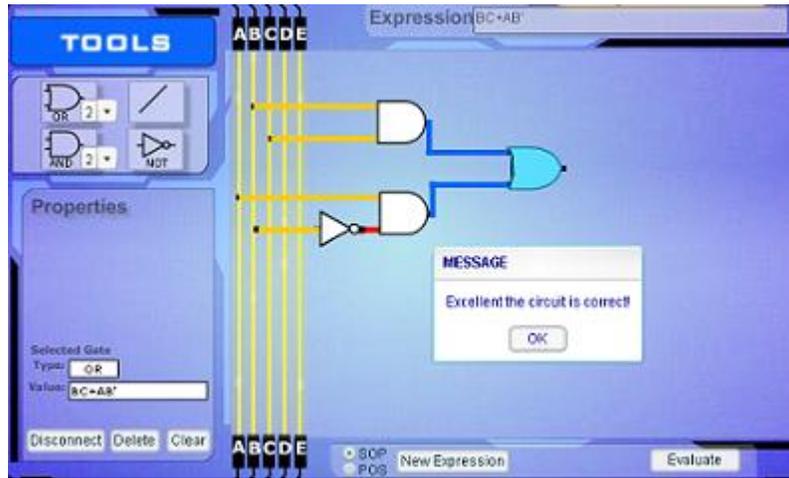
Figure 13: Final evaluated circuit design